Study of The Effect of different Dual insulator on Electrical and Bias Stability life Performance of a-IGZO TFTs

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Abstract

In the study, we fabricated a-IGZO thin film transistors (TFTs) with SiO2 and dual gate insulator SiO2/Al2O3, the thicknesses of SiO2/Al2O3 were 200/0 nm, 180/20 nm, 170/30 nm and 160/40 nm, respectively. The devices were annealing at 300℃ for one hour. After annealing, the results show that TFT with 170/30 nm SiO2/Al2O3 dual gate insulator display the best electrical performance compared to single SiO2 gate insulator based. The measured result show that saturation current, leakage current, insulator surface roughness, saturation mobility, threshold voltage, subthreshold swing (SS), Ion/Ioff ratio and the maximum density of surface states at the channel–insulator interface values obtained were 81.2 μA, 5.42x10-11 A/cm2, 2.95 nm, 7.86 cm2/V.s, 2.65 V, 0.19 V/dec, 4.31×1011 and 8.59×1011cm-2 respectively. We test device bias stability, the 170/30 nm SiO2/Al2O3 bilayer gate insulator device shows a substantially smaller threshold voltage shift of 0.98 V and -0.69 V after a 10 and -10 V gate voltage is applied for 1000s, and hysteresis ΔVTH shift 0.06 V. In addition, we measure the photo responsivity of IGZO TFT, the responsivity was 200 (A/W) with the illumination of 300 nm wavelength. Showing that IGZO has photosensitive properties and has the potential to be made into phototransistors.

Keywords--IGZO, Silicon (Si) doping, magnetron sputtering, thin film transistor, insulator, hysteresis, positive bias stress, negative bias stress, photoresponse.

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I. INTRODUCTION

With the rapid development of the technology industry, from the past cathode ray tube (CRT) to today's liquid crystal display (LCD), smart phones and next-generation displays, displays have been widely used in life. In recent years, Active-matrix organic light-emitting diode (AMOLED) displays using a metal oxide TFT have attracted much attention. The difference from passive structures used in the past is that the use of thin film transistors with capacitors to store signals, as electrical switching devices for turning pixels on and off, despite the higher cost and more complex technology, each pixel is continuously and independently drive and memorize the drive signals, which does not need to work under high pulse current, which improves the efficiency and extends the service life. Therefore, due to the development of technology, thin film transistors have attracted widespread attention in recent years, and people have increasingly higher requirements for the functions of displays to improve display technologies, such as high resolution, thin, low cost, low power consumption and large size also have furthered the development of thin film transistor technology. In the past TFT, the insulating layer SiO2 was used in the gate insulator. As the thickness of the gate dielectric layer of the device decreases, the SiO2 gate insulator will be affected by direct tunneling, resulting in a rapid increase in leakage current.

At present, high-k materials are used in the insulation layer to effectively suppress leakage current because they have high capacitance due to high dielectric constant. Therefore, double-layer insulation is used because the oxidation capacitance at the same thickness is lower than that of a single layer. The electrical constant can avoid reducing the mobility, and observe that the double insulation layer improves the electrical characteristics of the transistor of a single insulation layer [1].

II. EXPERIMENTAL PROCEDURES

This experiments are mainly distributed into some parts of step as shown in Figure. 1. Firstly, we commercially sintered IGZO target (1:1:1:4 mole%) with a diameter of 2” was used for the sputtering process. The substrate was a glass before facture the device, substrates were ultrasonically degreased by sequential treatment with trichloroethylene, acetone and methanol for 5 min each and then rinsed with deionized water to remove organic impurities. First the substrate was deposited Al electrode by thermal evaporation with a 70 nm. Then fabricated the gate insulators with SiO2/Al2O3 on glass substrate bottom-gate-type for a-IGZO TFTs. The 200, 180, 170, 160-nm SiO2 film as a gate dielectric layer was deposited by plasma enhanced chemical vapor deposition (PECVD) and the 40, 30, 20 nm Al2O3 as a gate dielectric layer was deposited by atomic layer deposition (ALD). The a-IGZO films with a thickness of 50 nm were deposited by RF-magnetron sputtering at room temperature using a target at input power 70 W. Base pressure before sputtering was 1x10-5 trorr and the oxygen partial pressure was used by argon and oxygen to kept pressure at a 10 mTorr in the chamber, and an RF power of 70 W was used. Finally, we used the thermal evaporation to deposited 70-nm Al as the source and drain (S/D) electrodes through the third shadow mask. Fig. 2 the different Dual insulator IGZO TFT devices schematic diagram is shown.

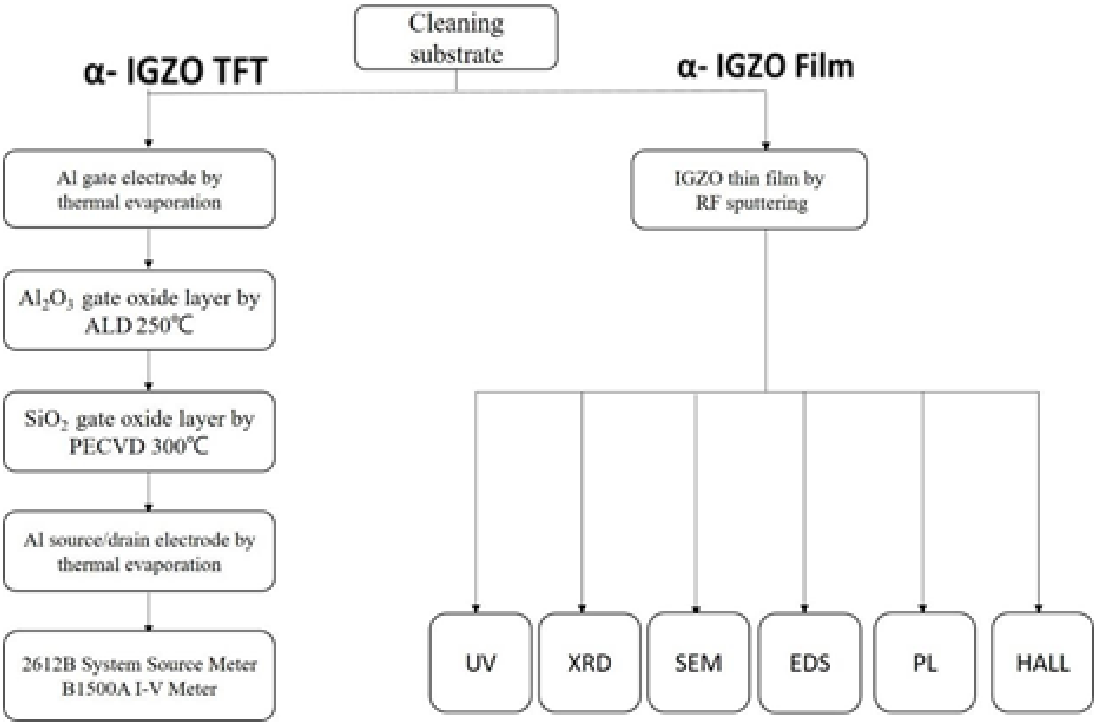

Fig. 1 Experimental process chart

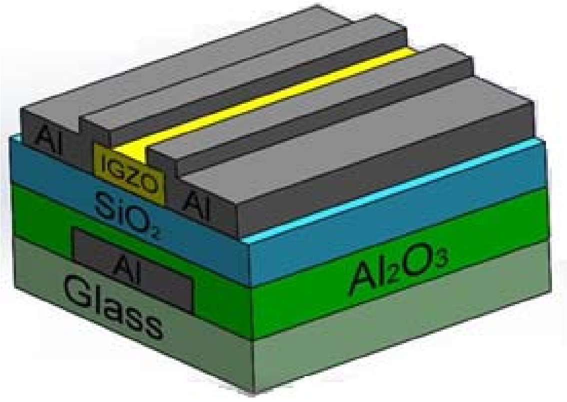

Fig. 2 IGZO TFT devices schematic diagram.

III. RESULTS AND DISCUSSION

Fig. 3 show the surface roughness images of SiO_2 film and SiO_2/Al_2O_3 bilayer film deposition on glass substrate, the root- mean-square (RMS) roughness of SiO_2 (200nm) film and SiO_2/Al_2O_3 (180/20, 170/30, 160/40nm) bilayer film are 3.65, 3.48, 2.95 and 3.12nm, respectively. The deposition of SiO_2 film on the Al_2O_3 film prevent from the damage of the Al_2O_3 surface by the process of sputtering IGZO film with high power and provide excellent template to growing IGZO film, the result show that the SiO_2/Al_2O_3bilayer insulator can reduce the roughness of SiO_2 film, and dense insulator can obtain less trap density of IGZO film and better insulator-channel interface [2]. When the carrier moves on smooth insulator-channel interface can reduce the scattering avoid to reduce mobility and low leakage current, increase the control ability of the gate.

Fig. 4 (A)-(D)Show the high dielectric constant material has a higher defect density than the low dielectric constant, trap-assisted tunneling a disadvantage that must be conquered when using high dielectric constant materials, via the AFM, we know that the surface of the insulation layer has indeed improved, so we do the measurement of the gate leakage current. Fig. 4 shows the leakage current characteristics of SiO_2 and SiO_2/Al_2O_3 bilayer insulator gate insulator obtained 200 nm-thick PECVD SiO_2 and 180,170,160 nm-thick PECVD SiO_2 / 20, 30, 40nm-thick ALD Al_2O_3 bilayer insulator, the leakage current values is 3.15 x 10^{-8}, 6.67 x 10^{-10}, 5.42 x 10^{-11} and 1.32 x 10^{-10} A/cm^2, respectively. Observed at V_{GS}= 8V. The 170nm-thick SiO_2/30 nm-thick Al_2O_3 bilayer insulator exhibits the lowest leakage properties, as it contains fewer impurities and is denser [3], it is confirmed that the leakage current can be reduced by the improvement of the insulator.

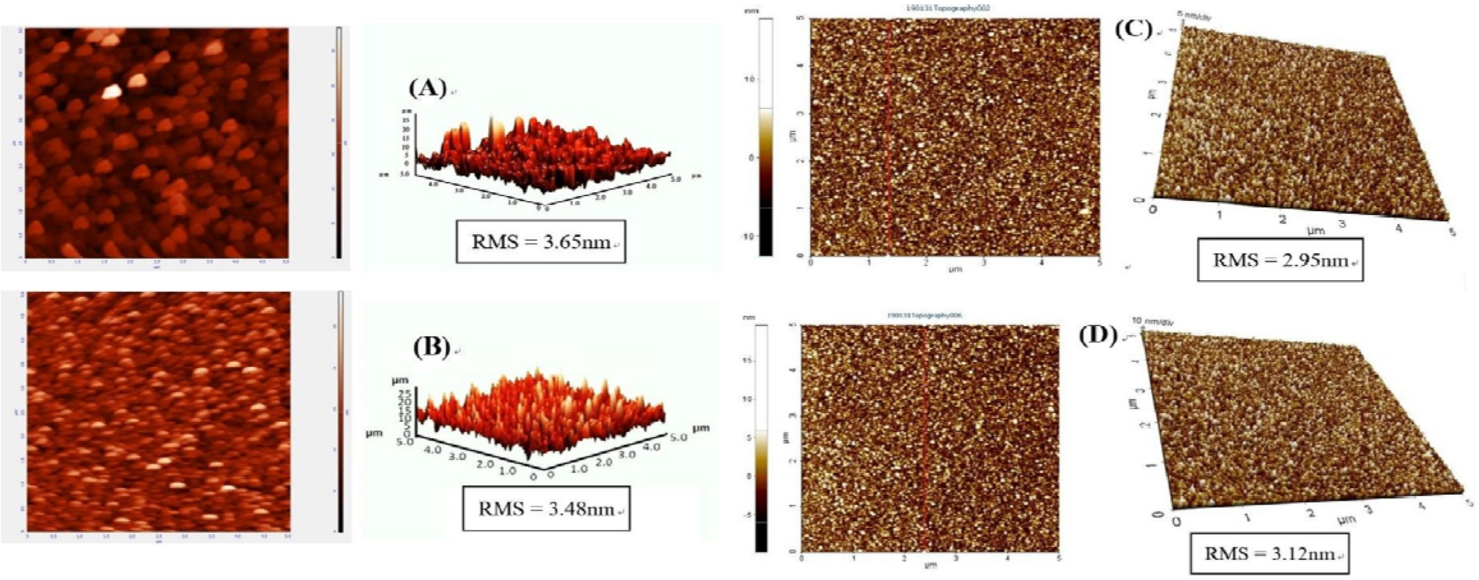

Fig. 3 AFM images of gate insulator(A) 200nm-SiO_2 (B)180/20nm-SiO_2/Al_2O_3 (C)170/30nm- SiO_2/Al_2O_3 (D)160/40nm- SiO_2/Al_2O_3.

Fig. 5(A)-(D) shows the output characteristics for the SiO_2 based TFT and SiO_2/Al_2O_3 based TFT, respectively. The drain current increased reach saturation with a gate voltage increased, according to our experimental results, the TFT with the 170nm-thick SiO_2/30 nm-thick Al_2O_3 bilayer gate insulator for IGZO TFTs has the exhibits high saturation drain current of 81.2 μA, were as IGZO TFTs with 200nm-thick SiO_2 gate insulator shows a comparatively low saturation drain current of 28.5 μA. Wherefore, it can be concluded that SiO_2/Al_2O_3 bilayer insulator can be improve trap at the junction of the channel and the insulator layer. All the devices have the n-channel enhancement mode because the electrons were generated by the positive VGS, there is no current crowding at the output characteristic of devices, indicating good ohmic contacts between the channel layer and source/drain metals. Fig. 6(a-d) shows the corresponding transfer characteristic I_{DS} versus V_{GS} and the $I_{DS}^{1/2}$-V_{GS} curves of devices. The devices parameters are recorded in Table. 1. In addition, Fig. 7(A)-(D) shows the capacitance–voltage (C-V) measurements was per- formed of 200 nm-thick PECVD SiO_2 and 180, 170, 160 nm-thick PECVD SiO_2 /20, 30, 40 nm-thick ALD Al_2O_3 bilayer insulator, which were Cox estimated to be about 0.19mF/m^2, 0.22mF/m^2, 0.26mF/m^2 and 0.31mF/m^2, respectively. We use Eq.1 to get g_m, the parameter it can be put into use Eq. 2 to calculate the mobility.

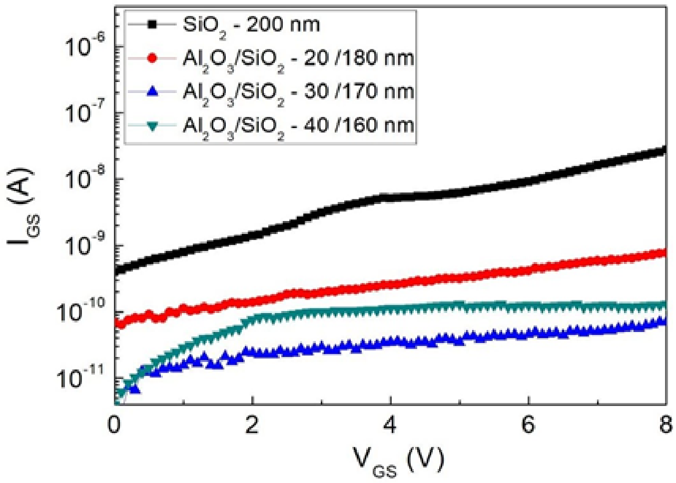

Fig. 4. Leakage current characteristics of IGZO-TFTs with difference insulators

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \qquad (1)$$

$$\mu_{FE} = \frac{L g_m}{W C_{ox}(V_{GS} - V_T)} \qquad (2)$$

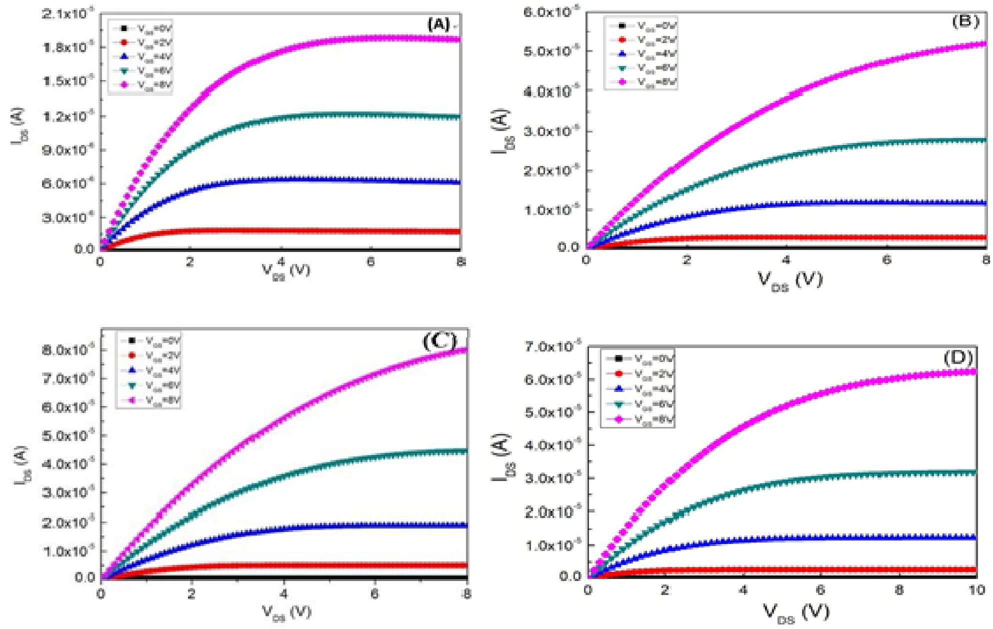

Fig. 5 Output characteristics of IGZO-TFTs with difference insulator(A) 200nm-SiO_2 (B)180/20nm-SiO_2/Al_2O_3 (C)170/30nm- SiO_2/Al_2O_3 (D)160/40nm- SiO_2/Al_2O_3

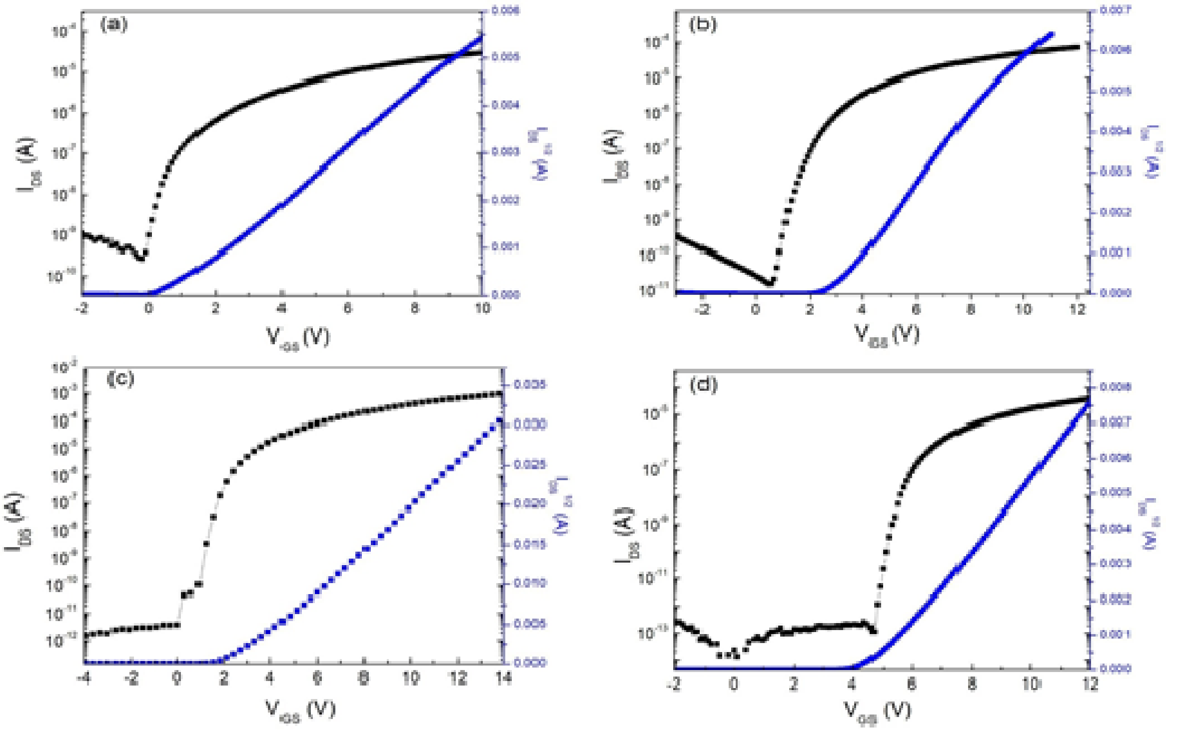

Fig. 6 The transfer characteristics of IGZO-TFTs with difference insulator(A) 200nm-SiO2 (B)180/20nm-SiO2/Al2O3 (C)170/30nm- SiO2/Al2O3 (D)160/40nm- SiO2/Al2O3

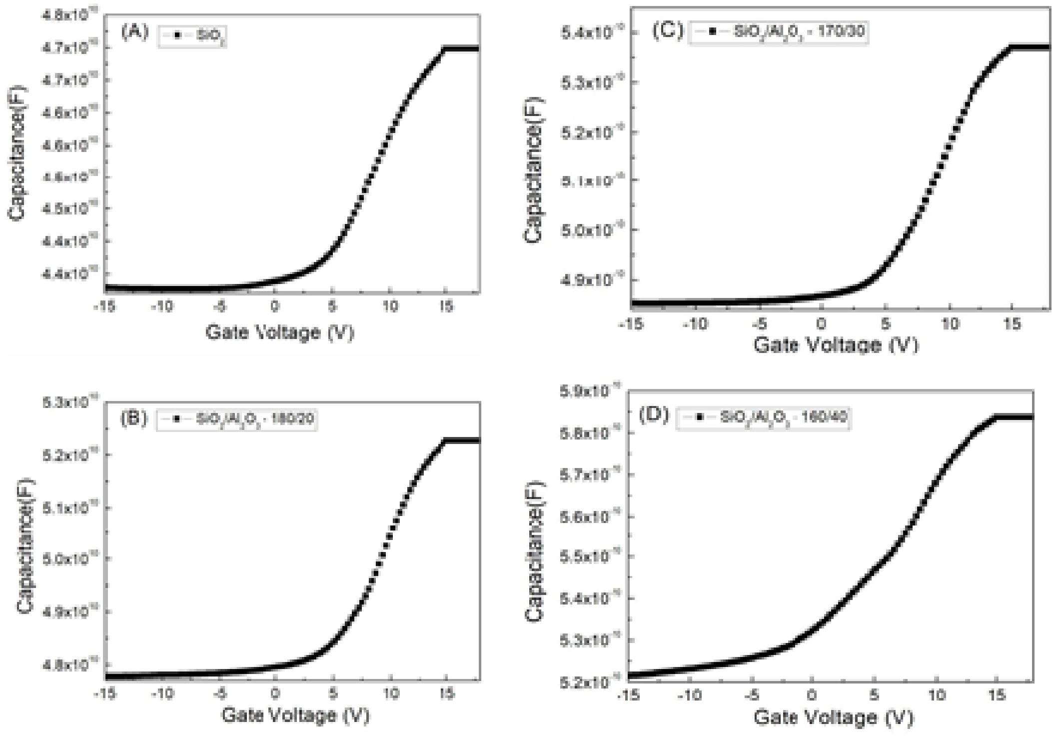

Fig. 7 Capacitance-voltage characteristics of IGZO-TFTs with difference insulator

Figs. 8 show the device hysteresis characteristics by measuring positive and negative voltage sweeps. When positive sweeps, electrons accumulate at the junction of the channel and the insulating layer, and electrons are trapped by the insulating layer defects of the junction, resulting in a larger voltage for the negative sweeps to make the device open. When the hysteresis of the IGZO TFTs with SiO_2 insulator is measured to be about 4.47V as shown in Fig. 8(A). Moreover, that a-IGZO TFT with SiO_2/Al_2O_3 bilayer gate insulator is measured to be about 0.86V, 0.06V and 0.49V, respectively. As shown in Fig. 8(B-D). Hysteresis phenomenon is observed when charges are trapped within gate insulator and at the interfaces between two layers. It is interesting to note that charge trap at the interface affects subthreshold swing while charge trap within gate insulator does not affects subthreshold swing as expressed by the following (Eq. 3) [4].

$$N_t = \left[\frac{S.S.\log(e)}{kt/q} - 1\right]\frac{C_{ox}}{q} \qquad (3)$$

We study the electrical characteristics of IGZO thin film transistors on the front side of different wavelengths of light, we use a xenon lamp of 550nm to 300nm interval 50nm as a light source to irradiate a wavelength. IGZO band gap 3.3eV converted to a wavelength of about 375nm, it is indicated that when the illumination wavelength is less than 375 nm, the oxygen vacancy (Vo) in the IGZO bulk is excited by the light energy to form an oxygen ion vacancy (Vo2+) and there will be obvious responsibility, it should remain unchanged under illumination from a source with a wavelength than 375 nm. However, we experimental results are not the case, we can observe that, when it is irradiated to a light source with a wavelength of 550 nm to 500 nm transistor has changed slightly. Guessing that defects or impurities in IGZO will have many energy states in the energy gap, the empty energy state is occupied by electron, when irradiate to light, the electrons gain energy and transition to the conduction Band, causing the IGZO conductivity to rise, the stronger the light energy excites the deeper energy level as shown in Fig. 9.[9-10] Due to illumination lead to subthreshold leakage and carrier concentration increase, the on-current and off-current of the transistor have an increasing trend, show that IGZO has photosensitive properties [11].

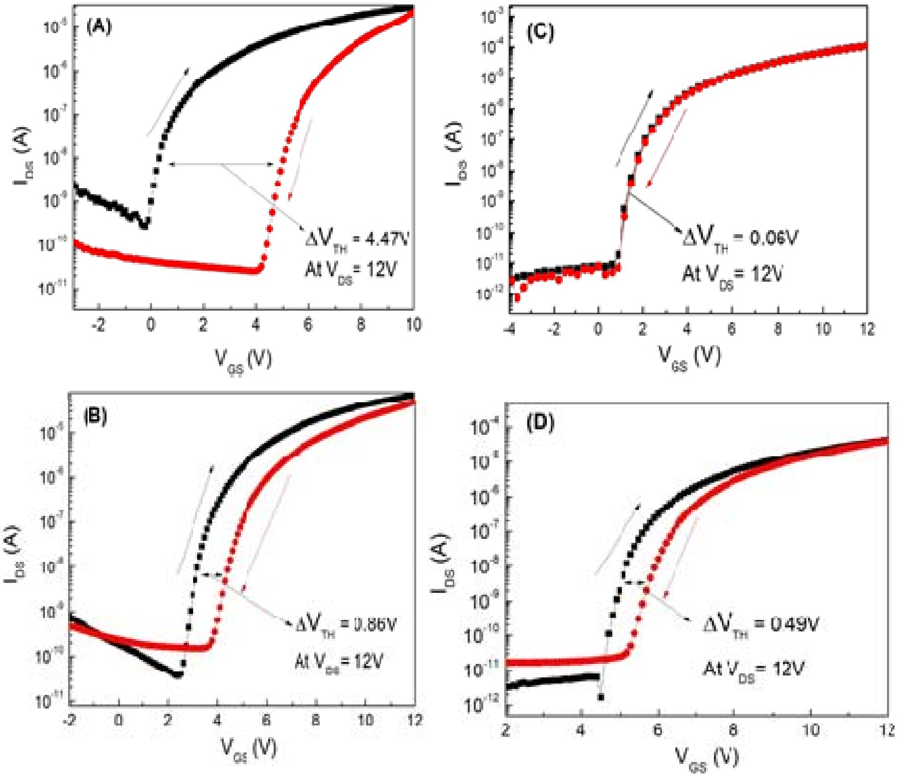

Fig. 8 Hysteresis characteristics curve of a-IGZO TFTs with (a) 200 nm - SiO_2 (b)180/20 nm - SiO_2/Al_2O_3 (c)170/30 nm - SiO_2/Al_2O_3 (d)160/40 nm- SiO_2/Al_2O_3

Table. 1 Transistor parameters of different insulating layers

Device	V_{TH} (V)	saturation current (μA)	Mobility (cm^2/V S)	Ion/Ioff ratio	S.S. (V/decade)	Nt (cm^{-2})
SiO_2 -200nm	0.86	28.5	9.25	1.12 x 10^5	0.98	4.982 x 10^{12}
SiO_2/Al_2O_3 -180/20nm	1.94	52.6	8.81	2.68 x 10^7	0.36	9.765 x 10^{11}
SiO_2/Al_2O_3 -170/30nm	2.65	81.2	7.86	4.31x 10^{11}	0.19	8.596 x 10^{10}
SiO_2/Al_2O_3 -160/40nm	4.76	63.6	6.91	3.35x 10^9	0.28	5.689 x 10^{11}

In order to understand the effect of electron beam generation on the characteristics of IGZO transistors, we will illuminate the front side of the device with ultraviolet light of 375 nm length and the gate bias of -15 V was applied for 1000 seconds, the characteristics are measured every 0, 200, 400, 600, 800 and 1000 seconds as shown in the Fig. 10, Because the IGZO band gap is 3.3ev, the ultraviolet light with a wavelength of 375 nm has sufficient energy to cause the electrons in the valence band transition to the conductive band to generate a large number of electron hole pairs. The gate applies a negative voltage, so the hole is attracted to the insulating layer by the influence of the negative bias, holes trapped into the insulation layer make the device easier to conduct, the threshold voltage offset negative direction. As shown in the Fig. 11[12].

Through the measurement results of different light wavelengths and negative bias illuminations stress, it can be found that the devices are greatly affected by light, especially at negative bias illuminations stress, the threshold voltage becomes larger in the negative bias illuminate at 400 seconds, indicates that the deterioration is serious. At 1000 seconds, due to the large number of electron hole pairs, the carrier concentration of IGZO is too high to form a conductive film make the device have no switching characteristics.

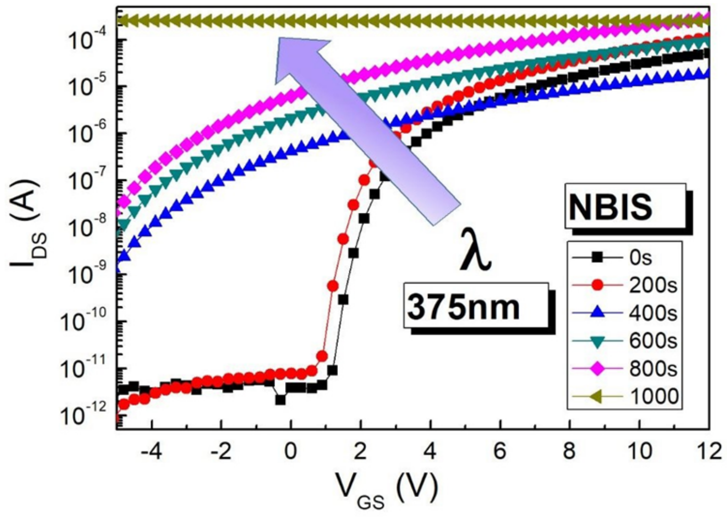

Fig. 10 The transfer characteristics during the negative bias illumination stress

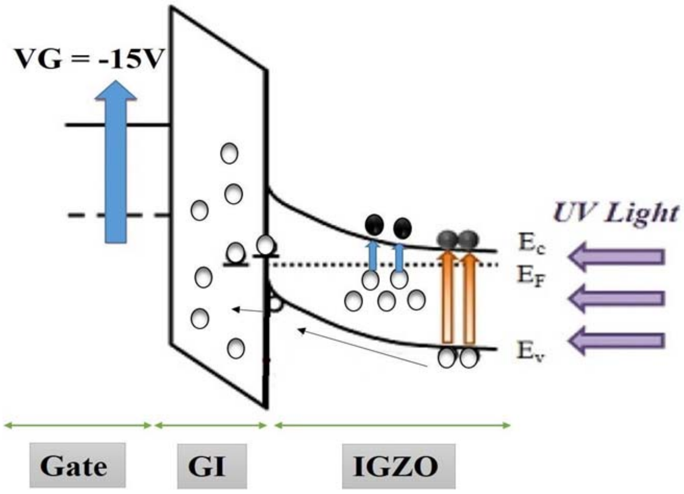

Fig. 11 Schematic diagram of the carrier being attracted to the insulating layer by NBIS

IV. CONCLUSIONS

We examined the electrical properties of the IGZO TFTs with SiO_2 insulator and SiO_2/Al_2O_3 bilayer insulator. The performances of the SiO_2 based TFT were improved after adding thin Al_2O_3 interlayer and their electrical characteristics, and bias voltage stress have been improved by comparing them to the IGZO-TFT with SiO_2 insulator. However, when the Al_2O_3 is increased to 40 nm, lead to trap-assisted tunneling leakage current to occur and the threshold voltage rises to 4.76V become the hard to open transistor. Therefore, we found that the TFF with the 170nm SiO_2/30nm Al_2O_3 bilayer insulator exhibited stabilized characteristics, the leakage current is 5.42 x 10^{-11}A/cm^2, the insulator surface roughness is 2.95nm, the hysteresis ΔV_{TH} is 0.06V, the PBS ΔV_{th} is 0.98V, the NBS ΔV_{th} is -0.69V, the saturation current 81.2μA, the saturation mobility is 7.86cm^2/Vs, the threshold voltage is 2.65V, the I_{on}/I_{off} ratio is 4.31×10^{11}, the subthreshold swing is 0.19V/dec and the maximum density of surface states at the channel–insulator interface is 8.59×10^{10}cm^{-2}. The SiO_2/Al_2O_3 bilayer insulator improves the insulator surface properties and leads to the high quality IGZO film and low trap density of IGZO /insulator interface.

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