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Evaluation of Y_2O_3 gate insulators thickness for α-IGZO thin film transistors

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Abstract

In this paper, Y_2O_3 was evaluated as a gate insulator for thin film transistors fabricated using an amorphous InGaZnO (α-IGZO) active layer. The leakage current density for the Y_2O_3 film prepared under the optimum conditions was observed to be ~1.5 × 10^{-8} A/ cm^2 at an electric field of 1 MV/cm. The RMS roughness of the Y_2O_3 film was improved from 0.330 nm to 0.216 nm by employing an RF (magnetron sputtering). Using the optimized Y_2O_3 deposition conditions, the IGZO thin film transistors (TFTs) were fabricated on a glass substrate. The optimal structure of the Y_2O_3/IGZO TFT was obtained.

Keywords: IGZO, Y_2O_3, RF magnetron sputtering, thin film transistor, self-heating effect.

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I. INTRODUCTION

With the rapid advancement of technology in recent years, displays have been widely used in life, from traditional CRTs to liquid crystal televisions (LCDs), flexible screens, and smartphones. Taking the smartphones manufactured by Samsung in South Korea as an example, the panel they use is Active Matrix Organic Light Emitting Display (AMOLED) technology, and the difference from the passive structure used in the past is: active The structure uses thin film transistor (TFT) and capacitor stored signals as an electrical conversion device to turn pixels on and off. Although the cost is more expensive and the technology is more complicated, each pixel can be driven continuously and independently. The driving signal can be memorized without the need to operate under high pulse current, the efficiency is improved, and the service life is also extended. Therefore, the thin film transistor as the core of its operation plays a pivotal role. Due to the development of technology, people have increasingly higher requirements on the functions of the display. In order to improve the technology of the display, such as high resolution, large size, light and thin, low cost, low power consumption, etc., it is undoubtedly starting from improving the characteristics of thin film transistors. A good choice has also promoted the vigorous development of thin film transistor technology [1].

Amorphous Indium Gallium Zine Oxide (α-IGZO) is one of many metal oxide semiconductors, and it has been widely used as an important role in the active layer of thin-film transistors in recent years. IGZO films are mostly made by RF magnetron sputtering process. It is divided into two methods for depositing films, one is co-sputtering method [2], which uses three kinds of In_2O_3, Ga_2O_3 and ZnO compound targets, by controlling the sputtering pressure, Sputtered wattage and gas ratio, etc. deposited thin film, in which zinc oxide is a n-type wide band gap semiconductor material of group II-IV, so zinc oxide can penetrate in the visible region and absorb in the ultraviolet region, with high carrier mobility , and can be processed in a low temperature environment. In order to improve its conductivity, it can be doped with impurities such as indium and gallium. Among them, indium mainly increases the electron concentration. The bond between indium and oxygen atoms is less stable than gallium. It is easy to generate oxygen vacancies and release electrons. As a semiconductor carrier, in order to have good stability and high On/Off ratio in application, you can choose to dope GaO with bonding stability, so that oxygen vacancies are not easily generated to reduce the carrier concentration ($<10^{15}cm^{-3}$) . However, indium gallium is an expensive and limited metal. In order to solve this problem, scientists use ZnO, which is quite mature in research, to mix. The ratio of $In_2O_3 : Ga_2O_3 : ZnO = 1 : 1 : 1$ is commonly used in academia and industry. Therefore, in this study, the target composition ratio of IGZO compound target is In_2O_3：Ga_2O_3：ZnO＝1：1：1 as the material of the active layer of thin film transistors [3][4].

II. EXPERIMENT

This experiment is mainly divided into two parts: the production of thin film transistors and the electrical measurement of thin film transistors. The flow chart of the experiment is shown in Figure 1. The thin film transistor produced in this experiment is a bottom gate structure [5]. We use a metal mask to define the shape of each layer of the thin film transistor, and use a thermal evaporation machine to deposit 70nm of aluminum as the gate, and use RF magnetron sputtering Plating (RF) yttrium oxide 220, 200, 180, 140nm as an insulating layer, then using RF Magnetron Sputtering to deposit the IGZO 50nm channel layer, and finally using a thermal evaporation machine to deposit 70nm aluminum The schematic diagram of the stacking of drain, source and transistor is shown in Figure 2.

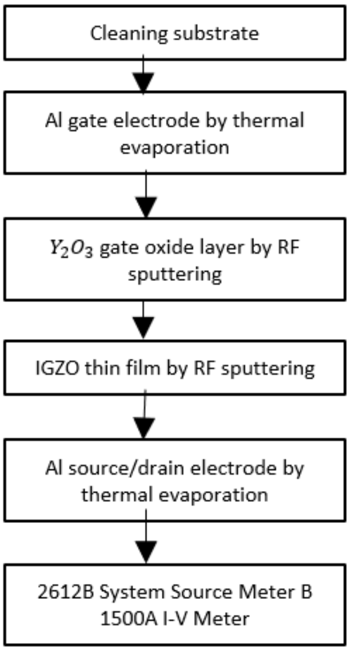


Figure 1. Experimental flow chart.

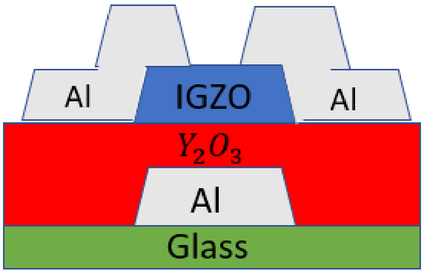


Figure 2. Schematic diagram of IGZO TFT with Y_2O_3 gate dielectric.

III. RESULTS AND DISCUSSIION

The dielectric constant of the Y_2O_3 film decreases with decreasing thickness, which not only affects the bandgap value, but also increases the proportion of the series capacitance caused by the interface layer when the thickness becomes thinner, and reduces the capacitance value C_{ox} of the entire oxide layer, if the oxide layer is too thin, there will be a problem of leakage current, the device will remain on. The proper thickness of the oxide layer can obtain the best conditions for opening and closing the device at room temperature. It has the lower energy barrier and the appropriate leakage current value for the device to close. The channel width (W) and length (L) are 1mm and 100um respectively. First, we name the thin film transistors with different conditions. The different thickness of the Y_2O_3 thin film is named a-d 220-140nm. Figure 3 (a-c) shows the output characteristics of the device when the gate voltage (VGS) = 10V is applied. The applied gate voltage (VGS) changes the drain current (ID) at increasing values of drain voltage (VD). Therefore, series of curves for the discrete values of VG can be obtained. Fig. 3(a-d) shows the output characteristic of IGZO channel TFT at the overlap length of 2μm with bottom gate (VGS) of 0 V increments of 2 V ranging from 0 V to +10 V. The graph shows active, pinch-off and saturation region and promising results with typical transistor theory. The operation revealed the fact that only a small drain current exists at VGS = 0 V generate carriers and tempted conducting channel with channel conductivity increased by positive VGS.

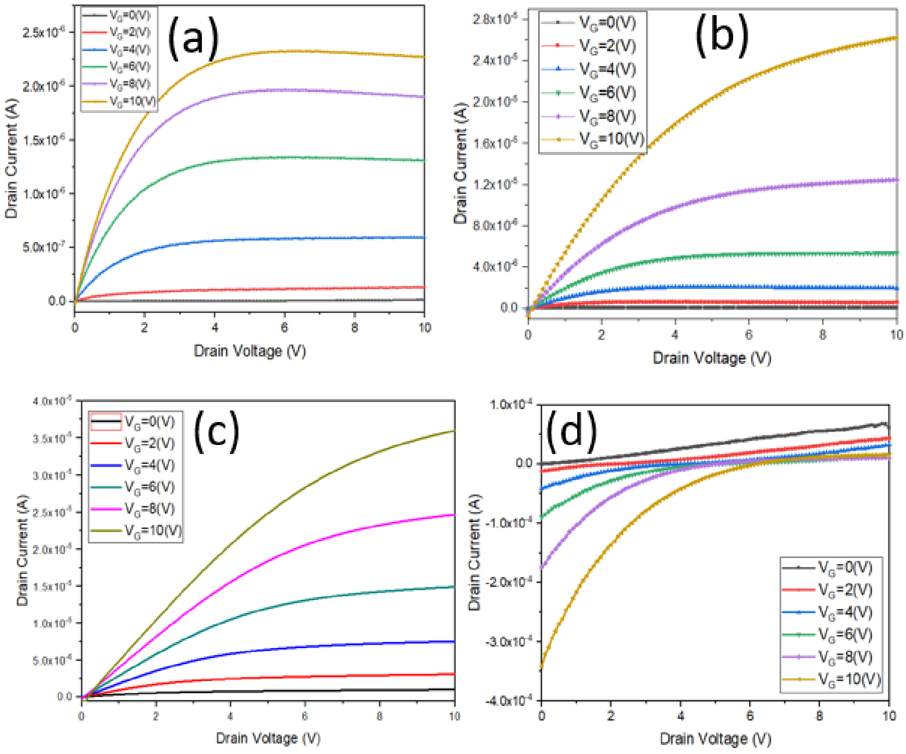


Figure 3. Output characteristics of IGZO-TFT with different Y_2O_3 thickness: （a） 220 （b） 200 （c） 180 nm （d） 140 nm.

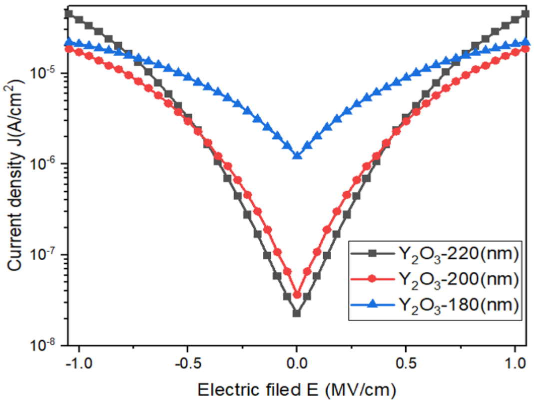


Figure 4. Leakage current density-electric field (J-E).

It can be seen from the graph that when the thickness is 220 nm, as shown in FIG. 3(a), the output characteristic curve (I_{DS}-V_{DS}) exhibits a self-heating effect, so the current at the drain will drop. The trend is mainly due to the poor thermal conductivity of the glass substrate on the insulating layer. In order to determine the problem of thermal conductivity on the glass substrate, we gave a heating source above the component and then re-measured. It was also found that the current dropped. Under high current, more Joule heat will be generated, and these Joule heat will accumulate in the channel layer because it is not easy to dissipate, causing lattice oscillation, so that the current will be reduced [6][7]. In Fig. 3(b, c), the I_D-V_D curve shows a very obvious behavior, and a pinch off region is formed. However, in Figure 3(b, c) and V_G=2V, there is a significant difference. This difference is because the substrate injection results in a lower total drain current [8], but it does not affect the overall operation of thin film transistors. In Fig. 3(c), it can be seen that when V_G=0V, there is a slight lack of alignment near 0(A), which may be due to the insufficient thickness of the insulating layer, which caused such a slight change. In order to prove that it is caused by the lack of thickness, in Fig. 3(D), it shows severe leakage current, and also loses the characteristics of the transistor, and the electric field-current density in Fig. 4 also shows the same situation. In the case of a thin film thickness, the insulating layer film usually exhibits fragile insulating properties caused by defects (such as pinholes). Therefore, the surface roughness values of thickness 220 and 180 nm were measured using (AFM) measurement as shown in Fig. 5. When the film thickness was reduced from 220 nm to 180 nm, the RMS values representing the numerical difference between the maximum and minimum points in the measurement range were estimated to be 0.216 and 0.330 nm, respectively. The 180nm thick film has a large RMS value, and due to the existence of many pinholes, it will cause a bad interface.

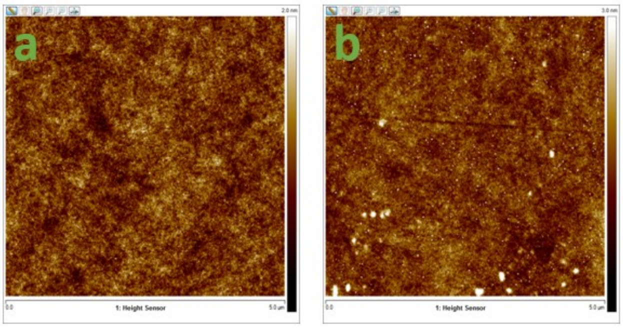


Figure 5. AFM image of the gate dielectric films: (a)220nm RMS(0.216nm), (b)180nm RMS(0.330nm).

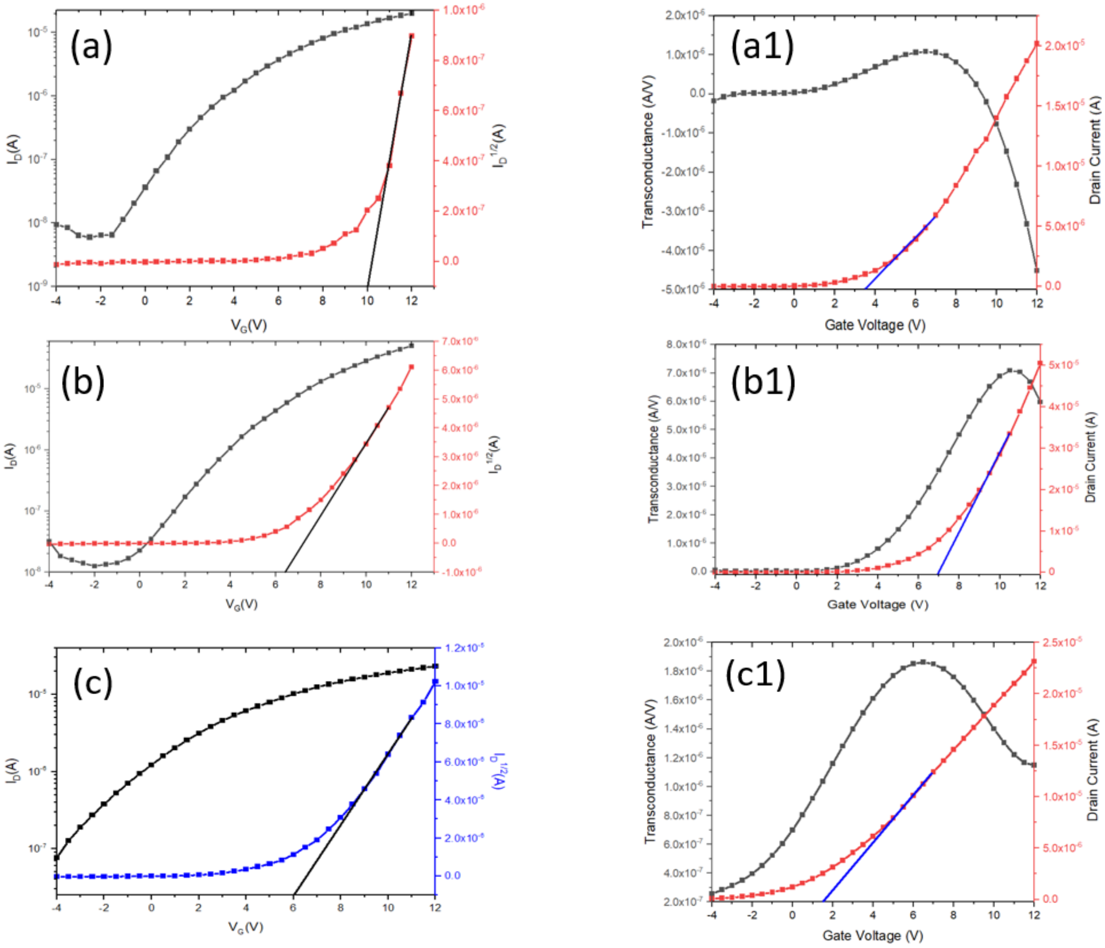


Figure 6. Transfer characteristic of α-IGZO TFTs with different Y_2O_3 thickness: （a,a1）220,（b,b1）200,（c,c1）180 nm.

Table 1. Electrical parameters of α-IGZO TFTs in this work

	V_t	SS	I_{on}/I_{off}	C_{ox}	u_{FE}	N_t	C(nF)
Y2O3-220nm	3.45	0.27	$4.4\text{x}10^3$	$4.7066\text{x}10^{-4}$	9.40	$1.0399\text{x}10^{16}$	5.648
Y2O3-200nm	6.45	0.31	$4\text{x}10^3$	$5.1773\text{x}10^{-4}$	42.2	$1.3596\text{x}10^{16}$	2.888
Y2O3-180nm	1.45	0.35	$3\text{x}10^2$	$5.7525\text{x}10^{-4}$	8.01	$1.7519\text{x}10^{16}$	2.876

From Fig. 6 (a-c and a1-c1), it is found that when the thickness of Y_2O_3 is 200nm, the value of V_t will be the maximum value [9][10][11], but the SS value will gradually decrease. The larger the value of SS, the smaller the change of I_{DS} with V_{GS}, and the current on-off characteristic is not obvious; the smaller the value of SS, the larger the change of I_{DS} with V_{GS}, the current on-off characteristic is significant, which can be observed in Table 1., when the thickness of Y_2O_3 increases, the values of μ_{sat} and SS do not decrease significantly. These results can be explained by the origin of simple electron trapping at the interface between the channel and the insulating layer. The most important electron mobility of thin film transistors is shown in Table 1. When the thickness is 200nm, u_{FE} will be the maximum value. It is speculated that Y_2O_3 is related to the IGZO thin film interface. From the study of A.H.Chen et al., it is easy to adsorb H_2O or CO_2 on the surface of Y_2O_3, forming Y-O-H or Y-O-C=O bonding, and when plating another film, the -OH or -C=O bond is broken due to the energy of external atoms, making Y-O form a dangling bond, easy to capture electrons , forming a leakage current [12], but those bonds containing H ions on the Y_2O_3 film will diffuse into the IGZO film, resulting in an abnormally high field effect mobility [13] because of the defect state of IGZO oxygen vacancies decreased, while the free electron concentration increased correspondingly. From the above comprehensive analysis, we can know that the Y_2O_3 film is very unstable in the atmosphere.

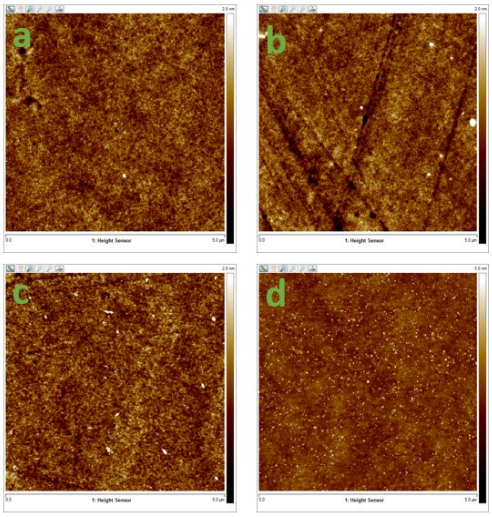


Figure 7. AFM image of the gate dielectric films: (a) today (RMS=0.22), (b) 1 day (RMS=0.26), (c) 4 days (RMS=0.296), (d) 7 days (RMS=0.397).

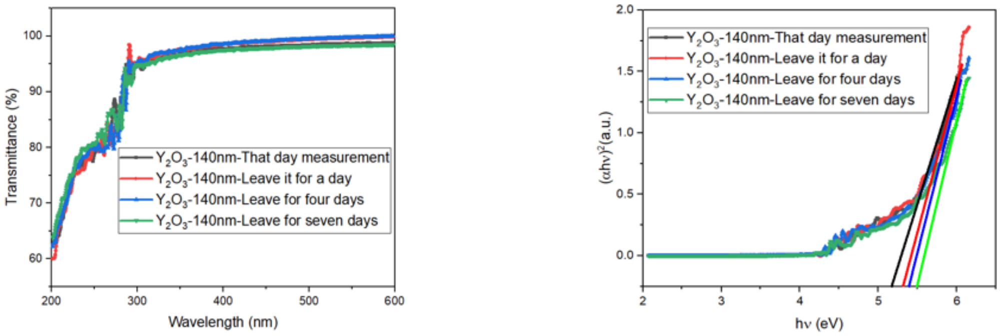


Figure 8. (Left) UV-vis transmittance spectra and (right) plot of $\alpha h\nu^2$ versus hv of Y_2O_3 (140nm).

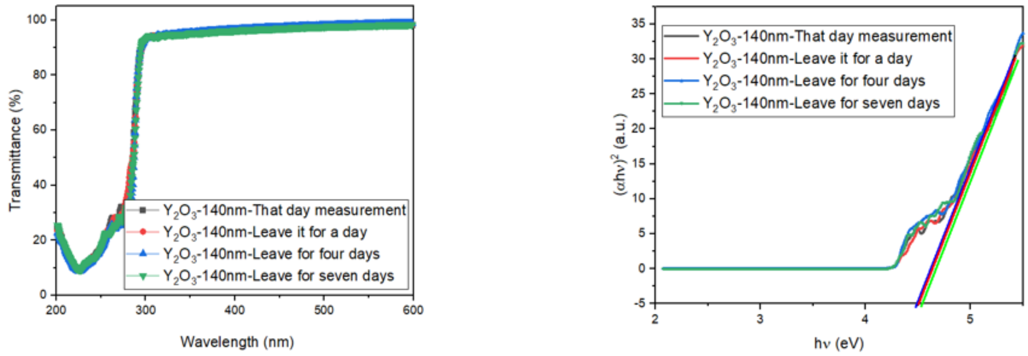
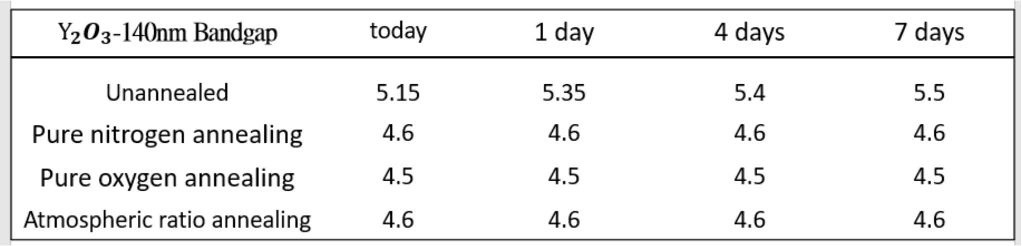


Figure 9. (Left) UV-vis transmittance spectra and (right) plot of $\alpha h\nu^2$ versus hv of annealed Y_2O_3 (140nm).

Table 2. Band gap (E_g) of Y_2O_3 placement time under different annealing conditions.



Y_2O_3-140nm Bandgap	today	1 day	4 days	7 days
Unannealed	5.15	5.35	5.4	5.5
Pure nitrogen annealing	4.6	4.6	4.6	4.6
Pure oxygen annealing	4.5	4.5	4.5	4.5
Atmospheric ratio annealing	4.6	4.6	4.6	4.6

Because Y_2O_3 film is not easy to store, it will cause damage to the component with the placement time, resulting in a reduction in the accuracy of the relevant data measured. Therefore, the above data are measured on the same day to ensure the accuracy of the experiment. We can know from the display in Figure 7 that with the increase of time, the surface of the film will become rougher. It can also be observed from the transmission spectrum in Figure 8 (left) that the fluctuations almost overlap, so it can be seen that the film thickness has little change with time, but the transmission spectrum is converted into an energy gap diagram through the formula. 8 (right) found that the 140nm film energy gap will increase significantly with time. In the same way, the penetration spectra of different annealing conditions are converted into energy gap diagrams and the observation of the penetration spectrum diagrams. Figure 9 (left: penetration spectrum diagram) and FIG. 9 (right: energy gap diagram) show the pure oxygen annealing related data. It can be seen from Figure 9 (left) that the thickness has not changed much. In Figure 9 (right), it can be found that the energy gap of the film after annealing does not appear to rise significantly with time, that is to say, the Y_2O_3 film can be annealed through annealing to extend the life, but after annealing, the energy gap of the film is also reduced some as shown in Table 2. In order to explain that annealing can prolong the life of the transistor, we use 200nm thick Y_2O_3 as the basis. From Figure 10 (unannealed), we can find that when this element is placed for seven days, the linear region and saturation current of the transistor are significantly different. On the contrary, as shown in Fig. 11 (annealed), it can be found that when this element is placed for seven days, the characteristics of the transistor hardly change, which shows that annealing can prolong the life of the transistor and also improve the adsorbed H_2O or CO_2 on the surface of Y_2O_3 with not annealed and increase I_D cut-off current.

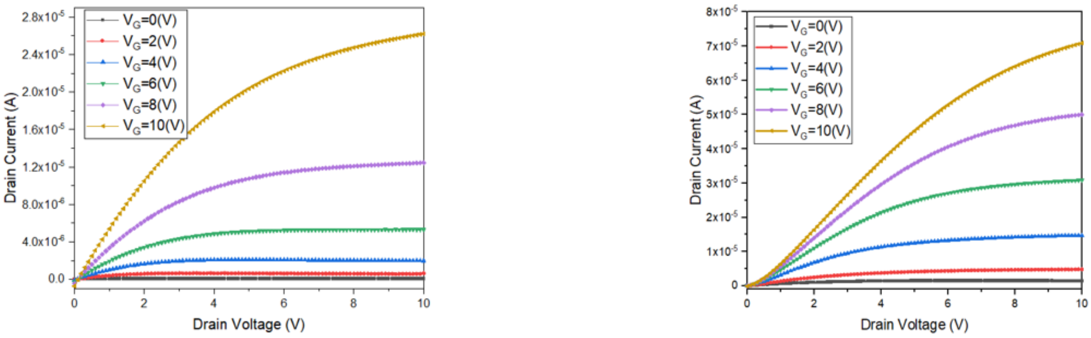


Figure 10. Output characteristics of IGZO-TFT with unannealed Y_2O_3 (left) measured on the day, (right) measured after being placed for seven days.

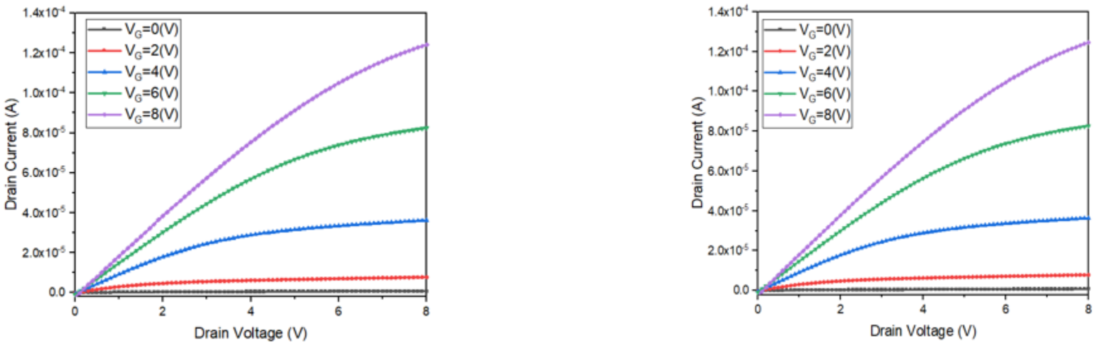


Figure 11. Output characteristics of IGZO-TFT with annealed Y_2O_3: (left) measured on the day, (right) measured after being placed for seven days.

IV. CONCLUSIONS

In this study, the optimal Y_2O_3 insulator structure of the IGZO TFT was 200 nm, which can form an enhanced n-channel transistor, the film has a transmittance of 91.30%, a suitable energy gap of 4.5eV, and a critical voltage of 6.45 V, I_{on}/I_{off} ratio is 4×10^3, the SS is 0.31V/dec, and the maximum surface energy state density at the channel-insulation layer interface is $1.3596\times10^{15}cm^{-2}$. However, after annealing this Y_2O_3/IGZO TFT, and then placing it for a week, this device can retain the transistor characteristics of a week ago, so after Y_2O_3 annealing, it can be more stable at room temperature, allowing the transistor to achieve the advantage of prolonged life.

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