Study of IGZO thin film transistors with Al_2O_3 gate insulator

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Abstract

In this study focuses on the dielectric layer materials of thin film transistors (TFTs). Gate oxide was deposited using a RF Magnetron Sputtering control system. The first studied the aluminium oxide (Al_2O_3) dielectric layer material deposited with different oxygen flow and annealed by the furnace tube. The study found that the properties of aluminium oxide (Al_2O_3) thin film transistors (TFTs) after furnace tube annealing reduced the interface trap density and the roughness of the thin film after annealing. The above dielectric layer is used to make thin film transistors (TFTs) with a bottom gate structure. The characteristics of thin film transistors (TFTs) are significantly improved by higher oxygen flow and additional thermal anneal. By analyzing the structure and electrical measurement of the thin film, the influence of the dielectric layer material on the thin film transistors (TFTs) is analyzed.

Keywords: Indium Gallium Zinc Oxide (IGZO), Thin Film Transistor (TFT), Al_2O_3

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I. INTRODUCTION

AMORPHOUS Indium-Gallium-Zinc-Oxide (a-IGZO) is a promising candidate for high performance TFT because it shows high field-effect mobility and on-current while has very low leakage current, and also, can secure uniform TFT characteristics when fabricated in large area.

Compared to silicon-based TFTs, a-IGZO TFTs have higher transparency over the entire visible range because they have wide band gaps. They also possess better uniformity than polysilicon TFTs because of their amorphous structure [1]. Because amorphous oxides have a more uniform structure and a smoother surface, this can result in a smooth channel interface with the gate insulator [2]. However, the problem of bias stability of a-IGZO TFTs gate bias stress still needs to be solved. According to many studies on the stability of a-IGZO TFTs, bias stability is very sensitive to oxygen vacancies in the a-IGZO film and to ambient oxygen molecules. For these reasons, passivation of oxygen vacancy defects and a-IGZO back channel layers are necessary to maintain good bias stability gate bias stress [1]. The deposition of oxide semiconductors is usually carried out by a simple sputtering method, and maintaining amorphous structure over a large substrate region is a major advantage of such materials [3].

	a-Si TFTs	*Poly-Si TFTs*	*Oxide TFTs*
V_{th} (V)	> 10V	<0.5V	<1V
Mobility (cm^2 /Vs)	<1	30-100	1-20
S.S. (V/dec)	< 0.5	0.2-0.3	~0.1
I_{on}/I_{off}	> 10^6	10^7	> 10^9
Light stability	Poor	Good	Superior to a-Si
Uniformity	Good	Poor	Good
Process Temp.(°C)	150–350	250–550	RT–400(600)
Cost	Low	High	Low
yield	High	Low	High

Table.1 The characteristics of a-Si, poly-Si and oxide TFTs [4,5,6,7,8].

As can be seen from the above Table.1, the advantages of oxide TFTs are not only high mobility, but also higher current than amorphous silicon (a-Si) TFTs. The oxide semiconductor has a leakage current of 1×1018A / um or less. For the ON/OFF ratio required for display performance, oxide thin-film transistors (TFTs) shows 109 or higher, which is polycrystalline silicon (107) 100 multiple. Although the mobility of In-Ga-Zn-O TFTs is lower than that of low-temperature poly-silicon (LTPS) TFTs, the fabrication cost is low and the uniformity is better than that of low-temperature poly-silicon (LTPS) TFTs, and large-area displays can be easily fabricated [7].

TFTs can change the structure and shape. TFTs of various structures and compositions can be easily modified or connected to other devices. Once the technical and cost challenges are solved, many new products using TFTs can be realized [4]. TFTs can also be made from a variety of semiconductor and dielectric materials, and variations in threshold voltage and mobility are still difficult to control due to material properties [4,10]. Current TFTs applications are mainly used for pixel driving of large-area LCDs. In large-size display production, display panels will require higher resolution and improved image quality, especially higher brightness, higher contrast, and more. Wide viewing angle and faster response time. Organic and oxide TFTs have been investigated as potential replacements for Si substrate TFTs to reduce production costs or improve mobility. In the near future, advances in TFTs technology may still be driven by the LCD industry [4,11].

II. EXPERIMENTAL DETAILS

In this study, the insulate layer and the active layer were both deposited by RF magnetron sputter system. We studied the effect of oxygen partial pressure (0sccm, 5sccm) on the properties of Al_2O_3 films under a fixed Ar flow rate and sputtering pressure, and studied the effect of annealing on Al_2O_3 films. The structure of Al_2O_3 deposited under different deposition and process conditions was obtained. Analyze the changes of Al_2O_3 thin film structure

and surface morphology, electrical characteristics and interface trap charge between IGZO semiconductors and the influence of TFT electrical characteristics.

200 nm Al_2O_3 was deposited as insulate layer of the thin film transistor by RF magnetron sputter system, at room temperature with the argon (Ar) gas and the oxygen (O2) gas were fed into the chamber, the working pressure of 10m Torr, the sputtering power of 200 W, and pre-sputtering is conducted for 10 min to remove impurities and to stability. After the sputtering, the film was annealed at 300°C for 1 hour in atmosphere by anneal furnace. The fabrication conditions are shown in Table.2 and Table.3. The metal mask was fixed on a substrate, 50 nm IGZO was deposited as channel layer of the thin film transistor by RF magnetron sputter system, at room temperature with the argon (Ar) gas at the flow rate of 95 sccm and the oxygen (O2) gas at the flow rate of 5 sccm were fed into the chamber, the chamber pressured of 10m Torr, the sputtering power of 70 W. After deposition of channel layer, the metal mask was fixed on a substrate to deposit 50 nm Al as source、drain of the thin film transistor, the channel length (L) of 3 mm and the channel width (W) of 4 mm by thermal evaporator.

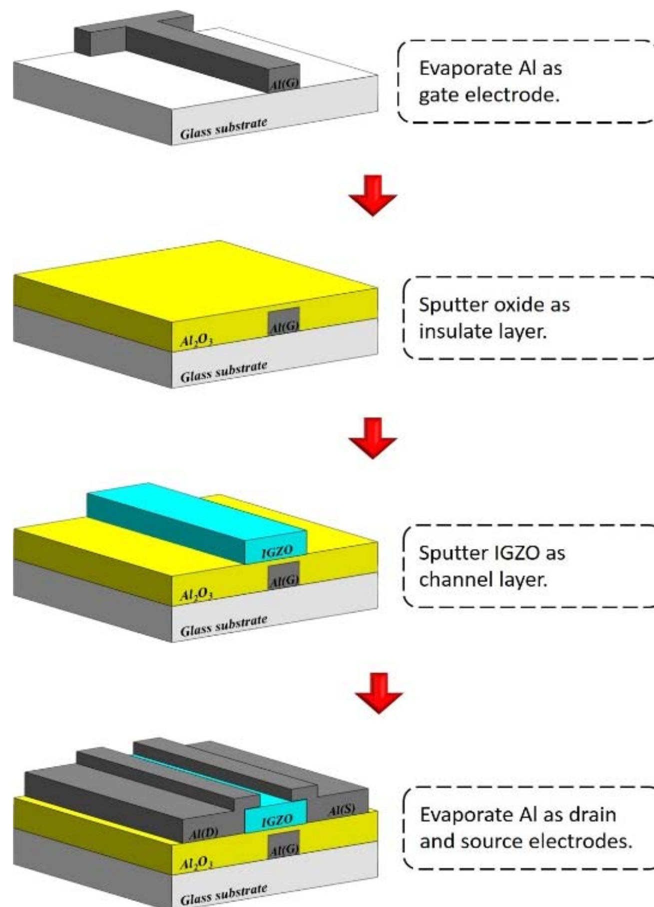

Fig. 1 The flow chart of device fabrication.

	Device A	*Device B*	*Device C*
Sputtering gas (Ar : O_2)	30:0 sccm	30:5 sccm	30:5 sccm
Annealing (Temp.)	No annealing	No annealing	Annealing (300°C)

Table. 2 Parameters of the insulate layer for devices.

Parameters	*Values*
Base pressure (Torr)	8 x 10^{-6}
Working pressure (mTorr)	10
Sputtering temperature (°C)	Room temperature
Ar : O_2 (sccm)	30:0 (Al_2O_3)、30:5 (Al_2O_3)、95:5 (IGZO)
RF power (W)	200 W (Al_2O_3)、70 W(IGZO)
Deposition rate (nm/min)	3.84 (30:0 sccm)、1.89 (30:5 sccm)、4.27 (IGZO)
Annealing temperature (°C)	300

Table. 3 Process parameters for the deposition of thin films.

III. RESULTS AND DISCUSSION

A. *Surface Analysis*

Fig.4 shows an AFM image of the surface morphology of Al_2O_3 films deposited on glass. The root mean square (RMS) roughness of the Al_2O_3 film of device A-C was 2.99, 2.03 and 1.64 nm, respectively. Because of the highest deposition rate in pure Ar, this limits the migration of sputtered atoms, resulting in a maximum surface roughness of the film. The addition of O2 gas begins to reduce the deposition rate, providing sufficient energy to improve its mobility on the substrate surface, resulting in dense, smooth, and less surface damage. Therefore, the RMS roughness can be reduced by adding oxygen [12,13,14]. The RMS of the deposited film after annealing at 300 ° C will decrease, which means that the film will become denser after annealing.

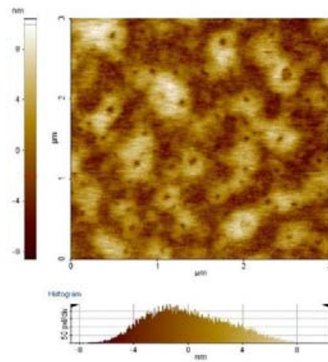

Fig. 2 AFM images of Device A.

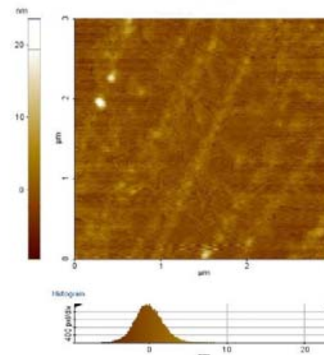

Fig. 3 AFM images of Device B.

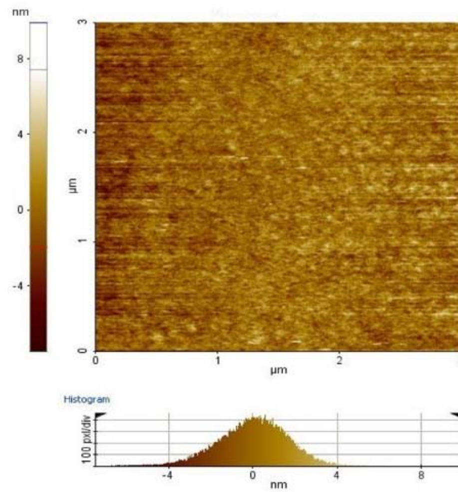

Fig.4 AFM images of Device C.

B. Leakage Current Measurement

The leakage current of the Al_2O_3 dielectric is shown in Fig.5 III. The leakage current of the Al_2O_3 film was 3.82×10^{-4} A, 3.14×10^{-4} A and 2.77×10^{-5} A. Al_2O_3 films are all amorphous films. It is beneficial to suppress leakage current caused by surface roughness. The leakage current in the film deposited under pure Ar and the O2 flow rate of 5 sccm was almost the same. Annealing at 300 °C improves the leakage current of the film. Because the Al_2O_3 film is subjected to an annealing process. Thermal annealing is an effective method to reduce this vacancy [15]. The annealed film improves the passivation of the interface state at the interface, delays the formation of charged defects at the interface, the decrease in leakage current indicates a reduction in defects in the film [16,17,18,19].

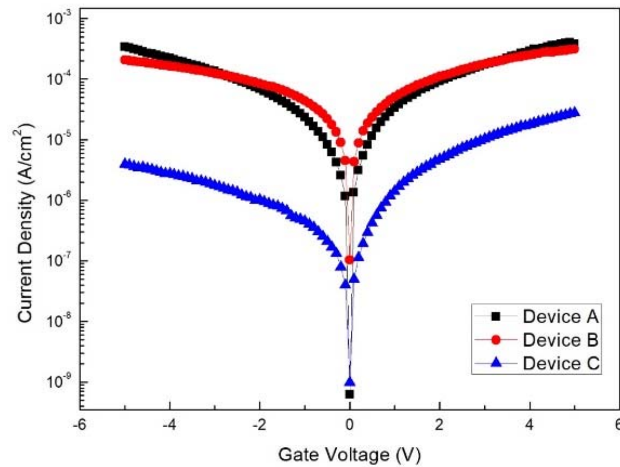

Fig.5 III The leakage current characteristics.

C. Elelectrical Characteristics of Devices

Fig. 6 shows the capacitance densities of the three gate dielectrics measured at a frequency of 100 kHz. They are 2.35、2.64、2.84 (nF/cm^2). As the flow of O_2 increases, the capacitance shows an increasing trend. After annealing, the device C shows the highest capacitance. The reduction in device A capacitance may be attributed to the porosity of the film deposition, which showed improvement after the film was annealed. This is due to the increase in film density [18].

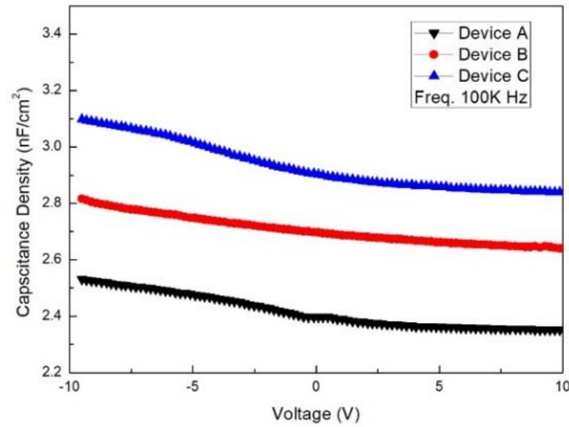

Fig. 6 Capacitance of devices.

D. Leakage Current Measurement

Fig.7 ~ Fig.9 shows the output characteristics of the TFTs with Al_2O_3 insulator different production methods, respectively, Showing a clear pinch-off behavior, all operating in the n-channel enhancement mode [15,20]. When the applied gate voltage (VGS) = 8 V and the source-to-drain voltage (VDS) = 10 V. The maximum saturation currents are 2.82×10^{-6} A, 1.61×10^{-5} A, and 2.61×10^{-5} A, respectively. Device C has the maximum saturation current because a smooth dielectric surface facilitates obtaining a smaller IGZO film trap density and a better dielectric /channel interface. The interface quality can be improved by reducing the interface trap density, to increase the saturation current of the device [21].

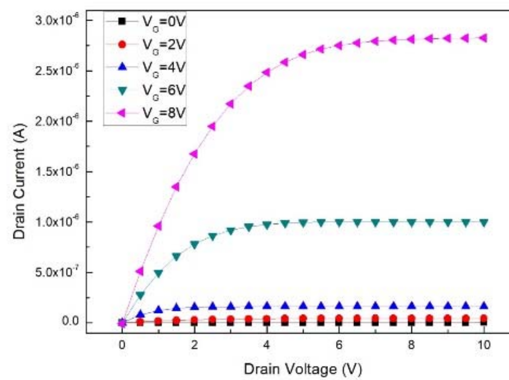

Fig. 7 Output characteristics of device A.

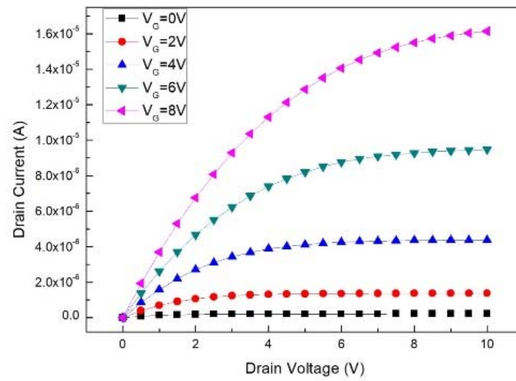

Fig.8 Output characteristics of device B.

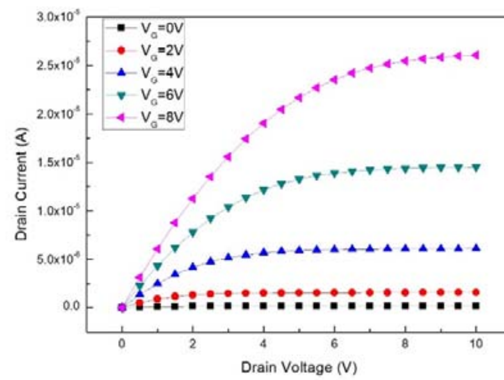

Fig.9 Output characteristics of device C.

To investigate the electrical performance of the device, Fig.10 ~ Fig.12 shows the transmission characteristics of all devices at a fixed drain voltage (VDS) = 10 V. The Vth of devices A, B, and C are 6.95, 6.14, and 4.18V, respectively. The calculated mobility of 0.81, 1.06, and 1.56 cm2/ Vs, respectively. The Ion / Ioff ratio of the device is approximately 8.23 x 104, 4.16 x 105, and 2.13 x 105, respectively. The S.S. values of the device were calculated to be 0.21, 0.17, and 0.11 V/decade, respectively. The calculated values of the trap density were 3.7 x 1010, 3.05 x 1010, and 1.5 x 1010 cm-2, respectively. Table.4 shows the Vth, mobility, Ion/Ioff ratio, S.S, and trap density for different devices.

	V_{th}(V)	mobility (cm^2/Vs)	S.S.(V /dec)	I_{on}/I_{off}	N_t(cm^{-2})
Device A	6.95	0.81	0.21	8.23×10^4	3.7×10^{10}
Device B	6.14	1.06	0.17	4.16×10^5	3.05×10^{10}
Device C	4.18	1.56	0.11	2.13×10^5	1.5×10^{10}

Table. 4 The electrical performance of the devices.

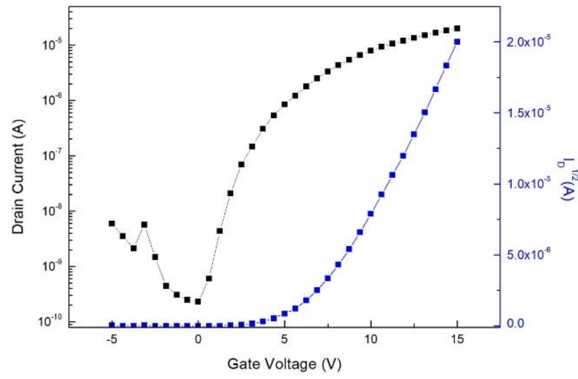

Fig.10 Transfer characteristics of device A.

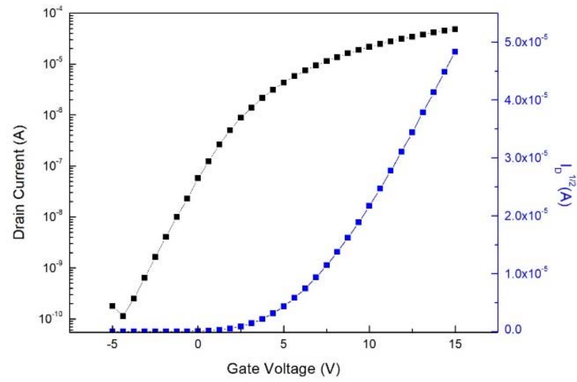

Fig.11 Transfer characteristics of device B.

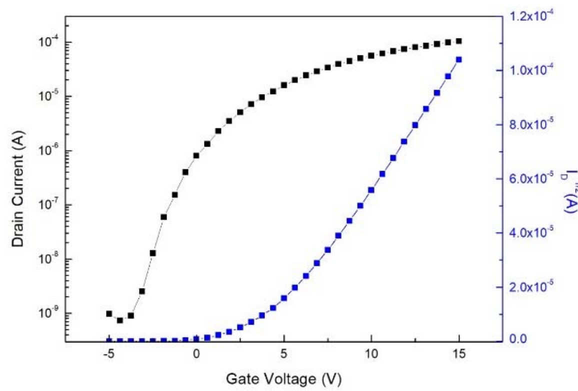

Fig.12 Transfer characteristics of device C.

Dielectric layer roughness is the main factor determining mobility [22]. Increasing roughness reduces mobility, smooth dielectric surfaces cause fewer interface defects, and a better channel- dielectric interface is obtained. Due to fewer interface defects and scattering centers, channel electrons are effectively suppressed, and electrons can be easily

transferred from the source electrode to the drain electrode in the channel. The smooth surface of the dielectric is also conducive to the growth of high-quality IGZO films [23,16,12,24]. Device A has more defects in the channel / dielectric interface and will capture more electrons during operation. Therefore, a larger Vth is required to turn on the device [16]. Device C achieved the smallest Vth. Because the defects including negative oxide charges generated during the sputtering process can be removed by annealing, the initial positive Vth shift caused by the negative oxide charges pre-existing in the dielectric can be reduced [25]. The highest Cox (2.84 nF/ cm2) was found after annealing. The increase of Cox leads to a decrease in Vth after annealing [26]. S.S. depends on the trap density at the interface between the channel and the gate dielectric. The improvement of S.S. indicates a decrease in interface state [27]. In addition, the switching current ratio (Ion / Ioff) of the TFT also increases with annealing, which is attributed to the decrease in Vth and the increase in mobility [28] .

IV. CONCLUSION

The experimental results show that a TFT using Al2O3 as a gate dielectric layer and IGZO as a channel layer was manufactured. There is no change in the film state of Al2O3 after annealing (no crystallization). Annealing has a denser effect, resulting in better film quality and lower surface roughness. It plays an important role in the device's mobility, Ion / Ioff ratio, subthreshold swing. After annealing, the TFT of the Al2O3 gate dielectric showed the best performance, the saturation current of 2.61 x 10-5 A, the threshold voltage of 4.18 V, mobility of 1.56 cm2 / Vs, an Ion / Ioff ratio of 2.13 x 105, the subthreshold swing of 0.11 V / decade and surface defects density Nt of 1.5 x 1010. As the surface state density at the channel-dielectric interface decreases, the dielectric interface is improved, smaller hysteresis changes are obtained, and the stability of the TFT is also improved.

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