# Design and Implementation of a High-Performance 79 GHz Up-Conversion Mixer in 90 nm CMOS

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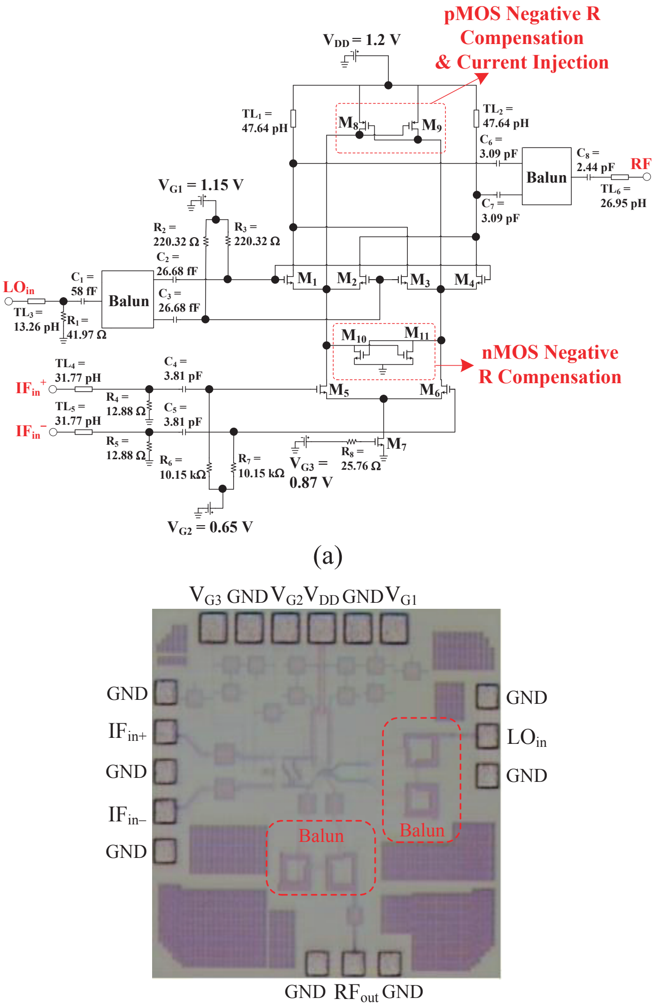
***Abstract*– A 79 GHz mixer for direct up-conversion using standard 90 nm CMOS technology is reported. The mixer comprises an enhanced double-balanced Gilbert cell with current injection for power consumption reduction, and dual negative resistance compensation for conversion gain (CG) enhancement, a Marchand balun for converting the single LO input signal to differential signal, and another Marchand balun for converting the differential RF output signal to single signal. The mixer consumes 13.6 mW and achieves IF-port input reflection coefficient ($S_{11}$) of –11.4 dB at 0.1 GHz, LO-port input reflection coefficient ($S_{22}$) of –12.2~ –28.7 dB for frequencies 75~90 GHz. At IF of 0.1 GHz and RF of 78.1 GHz, the mixer achieves CG of 2.1 dB and LO-RF isolation of 35.9 dB, the best CG and isolation results ever reported for a W-band CMOS/BiCMOS mixer with power consumption lower than 15 mW.**

***Index Terms*– CMOS, up-conversion mixer, conversion gain, Marchand balun, LO-RF isolation**

## I. INTRODUCTION

Recently, thanks to the rapid development of CMOS and SiGe processes, it has become possible to use them to implement 60 GHz wireless personal area network (WPAN) system and even 77 GHz radar system [1]-[5]. In transmitter design, the up-conversion mixer (or modulator) is a critical block which receives intermediate frequency (IF) signals, and then up-converts (or modulates) them by local oscillator (LO) signals to the whole RF band of interest. The basic requirements of a up-conversion mixer include good input impedance matching and LO-RF isolation, good output power and linearity, high conversion gain (CG) over the whole band of interest, and low power consumption.

To date, several excellent 60 GHz CMOS up-conversion mixers have been reported [6]-[7]. However, to our knowledge, there is no W-band (75~90 GHz) CMOS up-conversion mixer published in the literature (with power consumption lower than 15 mW), and there are only two reported W-band SiGe BiCMOS up-conversion mixers [8]-[9]. In [8], an 80 GHz SiGe BiCMOS Gilbert-cell based double-balanced up-conversion mixer with on-chip baluns at both RF and LO ports was demonstrated. Though high CG of 3.2 dB is achieved, its 104 mW power consumption and 21.4 dB LO-RF isolation is not good enough. In [9], an 80-GHz SiGe BiCMOS Gilbert-cell based double-balanced up-conversion mixer with multi-tanh triplet (N=3) transconductance stage was reported. Though excellent CG of 3.8 dB is achieved, its 107 mW power consumption and 21.1 dB LO-RF isolation is not satisfactory. To demonstrate that low-power, high CG, and excellent LO-RF isolation can be achieved simultaneously for a W-band CMOS up-conversion mixer using negative resistance compensation technique, in this work, we report a low-power 77~81 GHz up-conversion mixer with excellent CG and LO-RF isolation properties for short range automotive radars using 90 nm CMOS technology. The up-conversion mixer comprises an enhanced double-balanced Gilbert cell with current injection for power consumption reduction, and dual (NMOS and PMOS) negative resistance compensation for CG enhancement, and two Marchand baluns for converting the single LO input signal to differential signal, and the differential RF output signal to single signal.



(a)

(b)

Fig. 1 (a) Schematic diagram, and (b) chip micrograph of the 79 GHz CMOS up-conversion mixer.

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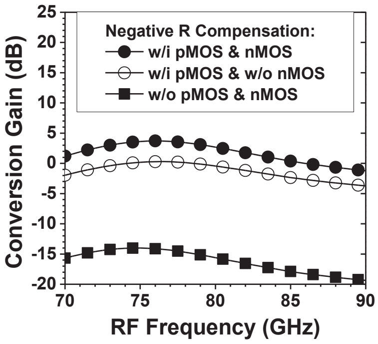
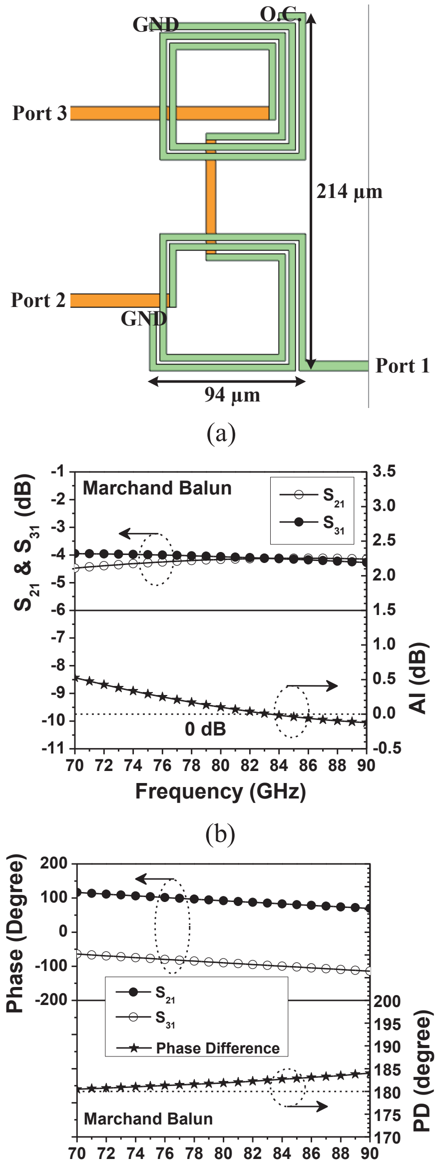


Fig. 2 Simulated CG versus frequency characteristics of the mixer at various conditions.



(a)

(b)

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Fig. 3 (a) Schematic diagram, and simulated (b) $S_{21}$ and $S_{31}$, and amplitude imbalance (AI), and (c) individual phase and phase difference (PD) of $S_{21}$ and $S_{31}$ of the Marchand balun.

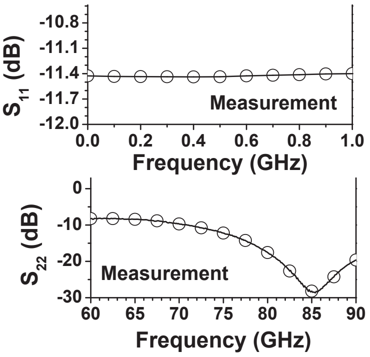

Fig. 4 Measured $S_{11}$ and $S_{22}$ versus frequency characteristics of the mixer.

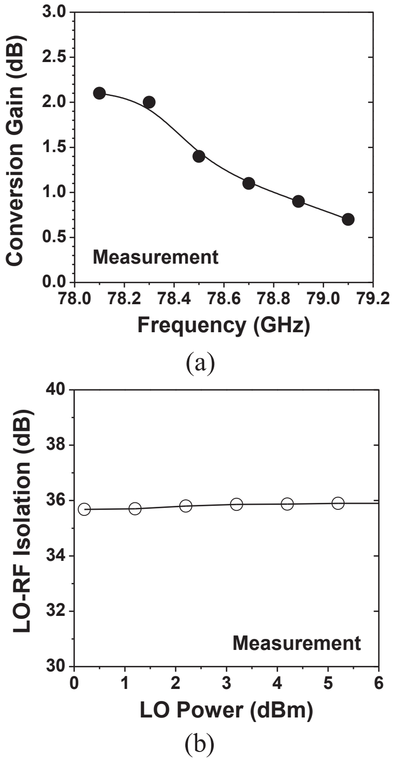

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Fig. 5 Measured (a) CG and (b) LO-RF isolation versus frequency characteristics of the mixer.

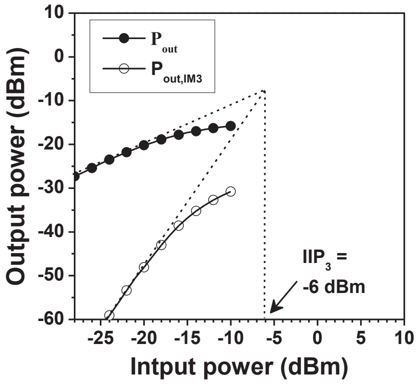

Fig. 6 Measured IIP3 of the CMOS up-conversion mixer at LO frequency of 79 GHz.

## II. CIRCUIT DESIGN

The 79 GHz up-conversion mixer was designed and implemented by a standard 90 nm CMOS process (on a p-type silicon substrate with thickness of 300 μm and resistivity of 8-12 Ω·cm) provided by a commercial foundry. This technology offers 9 metal layers, named $M_1$ to $M_9$ from bottom to top. The thickness of $M_9$ is 3.4 μm, and that of $M_8$, $M_7$~$M_2$, and $M_1$ is 0.85 μm, 0.31 μm, and 0.24 μm, respectively. The IMD (inter-metal dielectric) thickness is 0.74 μm between $M_9$ and $M_8$, 0.715 μm between $M_8$ and $M_7$, 0.32 μm between other adjacent metal layers, and 0.4 μm between $M_1$ and the first poly-silicon layer on the silicon substrate. The interconnection lines as well as the microstrip-line (MSL) inductors are implemented with the 3.4-μm-thick topmost metal to minimize the resistive loss.

Fig. 1(a) shows the schematic diagram of the CMOS up-conversion mixer. The up-conversion mixer comprises an enhanced double-balanced Gilbert cell, and two Marchand baluns. At DC, the pMOS cross-coupled transistors $M_8/M_9$ in the enhanced double-balanced Gilbert cell can inject current to the IF transconductance stage. This in turn results in a power consumption reduction and a linearity improvement of the mixer [10]. In addition, at AC, the pMOS cross-coupled transistors $M_8/M_9$ can provide an equivalent negative input transconductance $-g_{m8,9}$ at the source terminals of the LO switching transistors $M_1$~$M_4$. This in turn results in a CG enhancement of the mixer due to negative resistance compensation. To maximize the CG, note that a pair of nMOS cross-coupled transistors $M_{10}/M_{11}$ is also included in the enhanced double-balanced Gilbert cell for sufficient negative resistance compensation. Besides, the Marchand balun at the LO port is for converting the single LO input signal to differential signal, and the Marchand balun at the RF port is for converting the differential RF output signal to single signal. The other component parameters adopted are as follows: The gate-length is 0.1 μm for transistors $M_1$~$M_6$ and $M_8$~$M_{11}$, and 0.2 μm for transistor $M_7$. The gate-width-per-finger of transistors $M_1$~$M_4$ and $M_5$~$M_{11}$ is 3 μm and 5 μm, respectively. The finger-number of transistors $M_1$~$M_4$, $M_5$~$M_6$, $M_7$, $M_8$~$M_9$ and $M_{10}$~$M_{11}$ is 12, 45, 30, 24 and 3, respectively. In the bias condition of $V_{DD}$ = 1.2 V, $V_{G1}$ = 1.15 V, $V_{G2}$ = 0.65 V, and $V_{G3}$ = 0.87 V, the up-conversion mixer drains 11.3 mA current from the 1.2 V ($V_{DD}$) power supply, that is, the simulated power consumption is 13.6 mW. In addition, the simulated cut-off frequency ($f_T$) and maximum oscillation frequency ($f_{max}$) of the LO switching transistors $M_1$~$M_4$ are 128.4 GHz and 153 GHz, respectively. The good $f_T$ and $f_{max}$ performances indicate that it is possible to apply this CMOS process on the implementation of high-performance 79 GHz up-conversion mixer. The chip micrograph of the mixer is shown in Fig. 1(b). The chip area is only 0.724×0.827 $mm^2$ excluding the test pads.

Table 1 Summary of the implemented CMOS up-conversion mixer, and recently reported W-band up-conversion mixers.

| References | This Work | [8] | [9] |
|---|---|---|---|
| Topology | Gilbert-Cell with Dual Negative R Compensation | Gilbert-Cell with Output Buffers | Gilbert-Cell with Multi-Tanh Triplet $g_m$ stage and Buffers |
| RF Frequency (GHz) | 77~81 | 80 | 80 |
| IF Frequency (GHz) | 0.1 | 0.01 | 0.01 |
| CG (dB) | 2.1 (w/o buffer) | 3.2 | 3.8 |
| LO-RF Isolation (dB) | 35.9 | 21.4 | 21.1 |
| Power Consumption (mW) | 13.6 | 104 | 107 |
| Technology (nm) | 90 (CMOS) | 180 (BiCMOS) | 180 (BiCMOS) |

Fig. 2 shows the simulated CG versus RF frequency characteristics of the up-conversion mixer in various negative resistance compensation conditions. For the case with both pMOS and nMOS (dual) negative resistance compensation, the mixer achieves CG of 2.23~3.63 dB for frequencies 77~81 GHz, higher than that (CG of –0.79~ 0.27 dB for frequencies 77~81 GHz) for the case with pMOS negative resistance compensation only, and that (–16.1~ –14.4 dB for frequencies 77~81 GHz) for the case without both pMOS and nMOS negative resistance compensation. The reason why the negative resistance compensation can effectively improve CG of the up-conversion mixer is explained as follows: For the case without the negative resistance compensation, the CG of the mixer is given by

$$CG = \frac{2}{\pi} g_{m5,6}\omega_{RF}L \qquad (1)$$

in which $g_{m5,6}$ is the transconductance of the IF input transistors $M_5/M_6$, and L is the equivalent inductance of the load inductors $TL_1/TL_2$. On the other hand, for the case with the negative resistance compensation, the CG of the up-conversion mixer is given by

$$CG = \frac{2}{\pi}\frac{G_{m,LO}}{(G_{m,LO} - g_{m8,9} - g_{m10,11})} g_{m5,6}\omega_{RF}L \qquad (2)$$

in which $G_{m,LO}$ is the equivalent input conductance at the source terminals of the LO switching transistors $M_1/M_2$ (or $M_3/M_4$), and $-g_{m8,9}$ and $-g_{m10,11}$ is the equivalent input conductance of the cross-coupled transistors $M_8/M_9$ and $M_{10}/M_{11}$, respectively, for negative resistance compensation. Compare Eqs. (1) and (2), it is clear that CG can be improved by adopting the negative resistance compensation technique.

Fig. 3(a) shows the schematic diagram of the Marchand balun. The metal width and space are 4 μm and 2 μm, respectively. The balun consists of an unbalanced input (Port 1), an open terminal (O.C.), two short terminals (GND) and two balanced outputs (Port 2 and Port 3). Fig. 3(b) shows the simulated gains $S_{21}$ and $S_{31}$, and amplitude imbalance (AI) versus frequency characteristics of the Marchand balun. The simulated $S_{21}$ is equal to –4.17 dB at 79 GHz, and is larger than –4.28 dB for frequencies 75~85 GHz. The simulated $S_{31}$ is equal to –4.04 dB at 79 GHz, and is larger than –4.15 dB for frequencies 75~85 GHz. Besides, the simulated AI is 0.29 dB at 60 GHz, and is smaller than 0.29 dB for frequencies

75~85 GHz. Fig. 3(c) shows the simulated individual phase and phase difference (PD) of $S_{21}$ and $S_{31}$ of the Marchand balun. The simulated AI is $181.7^{o}$ at 79 GHz, and is equal to $181.1^{o}$~$182.8^{o}$ for frequencies 75~85 GHz.

## III. RESULTS AND DISCUSSIONS

On-wafer measurements were performed by an Agilent's 110 GHz RFIC measurement system. The mixer drains 11.3 mA current from a 1.2 V power supply, i.e., it consumes only 13.6 mW power. Fig. 4 shows the measured input reflection coefficients at IF-port ($S_{11}$) and LO-port ($S_{22}$) versus frequency characteristics of the mixer. The mixer achieves excellent $S_{11}$ of –11.43 dB at 0.1 GHz, and –11.4~ –11.44 dB for frequencies lower than 1 GHz. In addition, the mixer achieves excellent $S_{22}$ of –16.1 dB at 79 GHz, and –12.2~ –28.7 dB for frequencies 75~90 GHz.

Fig. 5(a) shows the measured CG versus RF frequency characteristics of the mixer. The mixer achieves CG of 2.1 dB at RF frequency of 78.1 GHz, close to that (3.4 dB) of the simulated one. In addition, the mixer achieves excellent CG of 0.7~2.1 dB for RF frequencies of 78.1~79.1 GHz. Fig. 5(b) shows the measured LO-RF isolation versus LO input power characteristics of the mixer at RF frequency of 79.1 GHz. The measured LO-RF isolation is 35.7 dB and 35.9 dB at LO input power of 0.2 dBm and 6.2 dBm, respectively. To characterize the non-linear behavior, two-tone IF signals with equal power levels and frequency difference of 10 MHz (i.e. 0.1 GHz and 0.11 GHz) were applied to the mixer. At LO frequency of 79 GHz, the measured input third-order inter-modulation point is –6 dBm (not shown here).

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Table I is a summary of the implemented CMOS up-conversion mixer, and recently reported state-of-the-art W-band SiGe BiCMOS up-conversion mixers. As can be seen, the mixer (without output buffers) achieves CG of 2.1 GHz, comparable to that (3.2 dB) of the mixer with output buffers in [8], and that (3.8 dB) of the mixer with output buffers in [9]. In addition, the mixer achieves the best LO-RF isolation and consumes the lowest power. The result indicates that the proposed up-conversion mixer with dual negative resistance compensation is promising for W-band RFIC applications.

## IIII. CONCLUSIONS

A low-power CMOS up-conversion mixer with high CG and excellent LO-RF isolation for 77~81 GHz short range automotive radar is reported. The state-of-the-art results of the proposed up-conversion mixer indicate that it is very suitable for W-band wireless communication systems.

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