Design of Low Power CMOS VCO Based on Current- Reused Topology for 10GHz Application

Meng-Ting Hsu*[a], Cheng-Chuan Chung[b], An-Cheng Ou[c]
hsumt@yuntech.edu.tw[a]
m10013219@yuntech.edu.tw[b]
m10113216@yuntech.edu.tw[c]

***Abstract* —In this paper, we present low phase noise and low power of the current-reused VCO with additional current reused circuit for 10GHz application. The power and phase noise can be reduced by proposed VCO. The VCO was implemented by the standard 0.18um CMOS process. Operated at 1.3 V, the VCO circuitry consumes 2.64 mW of power. The total chip size is 0.61 mm x 0.69 mm. The VCO tuning range covers from 9.33 GHz to 10.89 GHz . The measured phase noise at 1-MHz offset from 10.8 GHz is -108.39 dBc/Hz, which leads to an excellent Figure-of-Merit (FOM) of -184.8 dBc/Hz.**

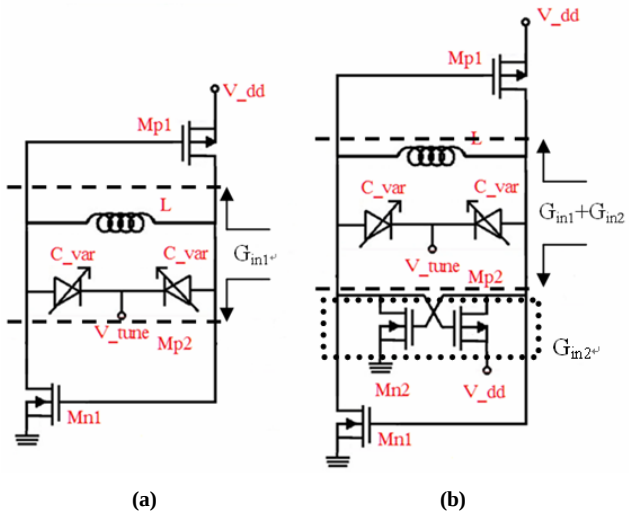
I. INTRODUCTION

During the past decade, the market for wireless communications requiring small, cheap, wide band, low phase noise and low power RF circuits has grown fast [1]. Voltage-controlled oscillators (VCOs) are one of the most important building blocks in these communications systems [2]. The major challenge lies in the design of fully integrated low phase noise and low power of voltage controlled oscillators (VCOs) that simultaneously have a wide tuning range. Recently, due to the rapid development and maturity of wireless communications and single-chip system integration, for the transmission of text, audio-visual, multimedia information and data, distance and time constraints can almost be ignored. All this will be due to the wireless communication technology improvement, wireless communication products has also been used in daily life, has brought many conveniences for human life.

Based on the literature, the circuit structure of the current-reused oscillator has lower power consumption compared to that of the conventional LC-VCO at 10 GHz operating frequency [3]. At higher operation frequency, the oscillator usually needs large bias current to provide enough transconductance (gm) [2]. This paper presents a new structure to investigate how to reduce power with fine phase noise at 10 GHz operating frequency. This paper is organized as follows. In section II, the design of a low power twin current reused VCO circuit topology is proposed. The comparisons of power and phase noise are evaluated by simulation. In section III, the measured results of the proposed VCO. The comparisons of the circuit performance are also described. Finally, the conclusions are in section IV.

II. CIRCUIT DESIGN

A widely known oscillator is the conventional differential negative -g_m oscillator that is shown in Fig.1(a) [4]. The topology consists of P-N current reused, inductors and two varactors. The proposed VCO with n-MOS and p-MOS current reused circuit in Fig.1(b). M_{p1}, M_{p2} and M_{n1}, M_{n2} using cross connection is to produce negative resistance for compensation the parasitic resistance of LC-tank. In order to verify the proposed additional current step closer recycling circuit has a better performance by circuit simulation to demonstrate with optimization phase noise and low power consumption characteristics.



s

Fig. 1 (a) Conventional current reused VCO, (b) The proposed VCO with additional current reused structure

When the oscillation frequency and supply voltage are at the same condition with 10.4 GHz and 1.3 V, respectively. The proposed VCO has better phase noise performance than the traditional current reused VCO. Fig.2 shows the phase noise property between with and without additional current reused circuit. The difference of phase noise between both VCOs is about -7.313 dBc/Hz at 1 MHz offset. Therefore, the phase noise can be improved with the help of additional current reused circuit. In power consumption part is shown in Fig.3, if the phase noise of both VCO is setting -114 dBc/Hz under the same voltage 1.3 V, then the difference of the total power consumption is about 6.77 mW at control

Corresponding author:hsumt@yuntech.edu.tw
DOI:10.6159/IJSE.2014.(4-1).70

voltage 0.5 V (including the same buffer).

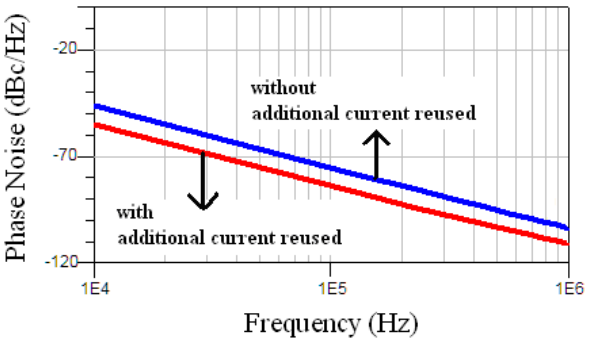


Fig. 2 Simulation the difference of phase noise.

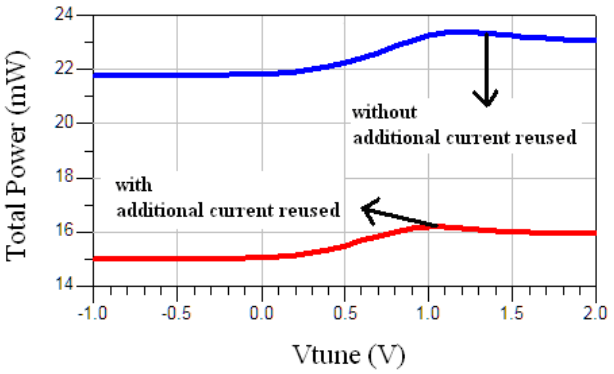


Fig. 3 Simulation the difference of power consumption.

A. Current Reused Topology with Additional P-N Current Reused Structure

In Fig. 4, we can analyze several important parts of equivalent circuit of proposed VCO. The left side is the LC tank and the right side is the active circuit.

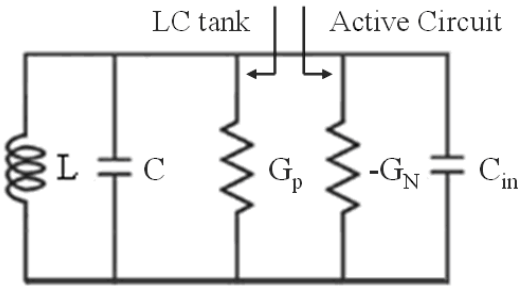


Fig. 4 Equivalent circuit of proposed VCO.

The tank circuit consists of an inductor with high Q value (Q=14) and varactor components. The model values for the inductor and varactor are selected to control oscillatory frequency. Gp denotes the passive element loss of LC tank.

An active circuit is used to provide negative resistance ($-G_N$) and compensate for the loss of the LC tank. In Fig.1(a), we can obtain the input conductance G_{in1} with low frequency model by the following equation:

$$G_{in1} = -\left(g_{mp1} + g_{mn1}\right) \quad (1)$$

If Gp denotes the passive element loss of the LC tank, then the start-up condition for oscillation is the following:

$$G_p + G_{in1} \le 0 \quad (2)$$

The proposed current-reused VCO is with an additional P-N current reused structure, the transistors M_{n2} and M_{p2} of input conductance G_{in2} can be reduced as follows:

$$G_{in2} = -\left(g_{mp2} + g_{mn2}\right) \quad (3)$$

The start-up condition of proposed VCO becomes the following equation:

$$G_p + (G_{in1} + G_{in2}) \le 0 \quad (4)$$

And oscillation frequency is $\omega_0 = \left(\sqrt{L(C + C_{in})}\right)^{-1}$.

General current-reused VCO that is used to generate a negative resistance by NMOS and PMOS transistors are shown in Fig. 5(a). They are shown with the output between the ends of LC tank, and thus result in a stable frequency of oscillation. However, this architecture of the VCO cannot be an ideal balance for the voltage swing. Concerning the output voltage for the positive half period that was shown in Fig. 5(b), the MN1 and MP1 transistors are the ON state, which can result in large current flows through the MN1 and MP1 transistors. At the DC condition, we can obtain the capacitance of the X/Y node as $C_x = C / 2 + C_{px}$ and $C_y = C / 2 + C_{py}$ (C_{px} / C_{py} is the parasitic capacitance of the X node and Y node to ground, respectively). If the output voltage of the negative half period that is shown in Fig. 5(c), then M_{p1} and M_{n1} are all in the OFF state.

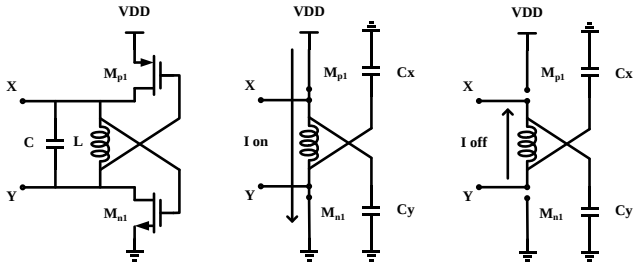


Fig.5 (a) Current reused VCO oscillation mode (b) Equivalent circuit of positive half period (c) Equivalent circuit of negative half period.

III. MEASURED RESULT

The proposed VCO is fabricated by TSMC 0.18um 1P6M CMOS technology. Fig.6. shows the die micrograph of the proposed 10 GHz low power consumption VCO, which cost a chip area of 0.61×0.69 mm^2. Fig.7 shows the output spectrum of proposed VCO which operated frequency is 10.8 GHz with -5.23 dBm peak value. Fig.8 shows the tuning ranges of the oscillation frequency versus varactor controlled voltage (Vtune) which is tuned from 0 V to 2 V. The proposed VCO operated between 9.33 GHz and 10.89 GHz, achieved 15% and 1.56 GHz tuned-range. The phase noise is -108.39 dBc/HZ at 1MHz offset frequency from 10.8 GHz in Fig.9. The measured power of the core circuit is 2.64 mW. The general performance with comparison FOM of VCO is defined as following [10] :

$$FOM = L\{\Delta f\} - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P}{1mW}\right) \quad (5)$$

$$FOM_T = FOM - 20\log\frac{FTR(\%)}{10} \quad (6)$$

$L\{\Delta f\}$ is indicated as the phase noise at Δf offset from the carrier f_0 and P is the core power dissipation. The comparison of 10 GHz VCOs are summary in Table I. Most of the VCOs have high FOM more than -180 dBc/Hz. Focusing on core power dissipation of VCOs, our work shows good performance for low power applications.

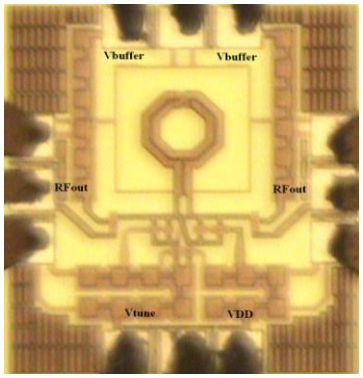


Fig. 6 Chip photograph of the proposed VCO.

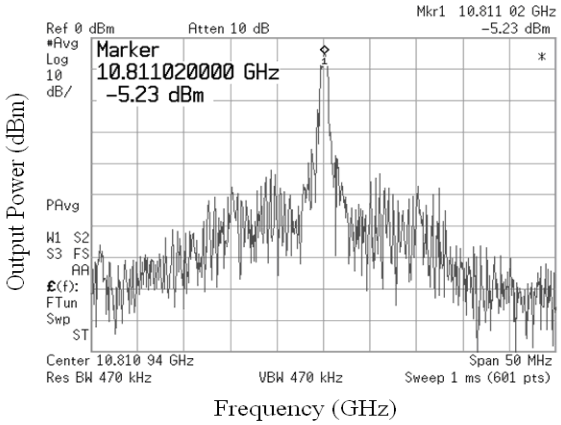


Fig. 7 Output spectrum of the proposed VCO at 10.8 GHz.

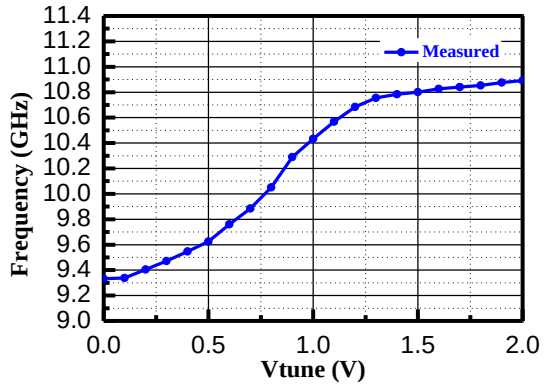


Fig. 8 Output oscillation frequency versus control voltage of proposed VCO.

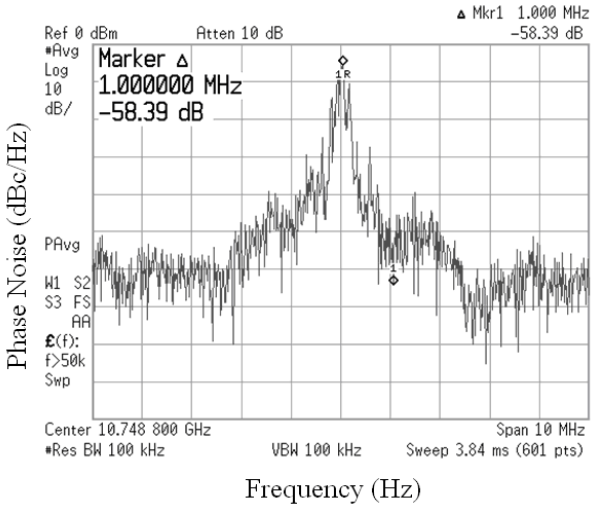


Fig. 9 Measured phase noise of proposed VCO.

TABLE I
THE PERCENTAGE OF ILL-CONDITIONED LMVS

Ref.	F(GHz)	Tuning Range (%)	Phase Noise	Core Power (mW)	FOM	FOMT *
This work	10.8	15	-108.4	2.64	-184.8	-188.3
[5]	10	20	-125	50	-188	-194
[6]	10	12	-108	7.2	-176.4	-177.9
[7]	10	16	-118	22.4	-184.5	-188.5
[8]	10.19	16.1	-105.2	3	-181.6	-185.5
[9]	10.1	6.4	-106.9	2.88	-182.4	-178.5

IV. CONCLUSION

A 10 GHz current-reused CMOS VCO is presented for low phase noise and low power consumption. The proposed low power VCO is fabricated by 0.18um CMOS process. The measurement results show that the phase noise -108.39 dBc/Hz at 1 MHz offset frequency and output power about -5.23 dBm. Measured tuning range is about 15% from 9.33 GHz to 10.89 GHz and power dissipation is 2.64 mW. The FOM of the VCO is about –184.8 dBc/Hz.

ACKNOWLEDGMENTS

The authors would like to thank the Taiwan Semiconductor Manufacture Company (TSMC) and National Chip Implementation Center (CIC) for the wafer fabrications and IC measurement. The project was partly supported by National Science Council (NSC 101-2221-E-224-049).

References

[1] Craninckx, Michiel S. J. Steyaert, “A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors,” Solid-State Circuits, IEEE Journal of Volume 32, Issue 5, May 1997 Page(s):736 – 744.

[2] Zhongtao Fu, Anand Pappu, Alyssa Apsel, “Beating the power limit of LC oscillators, ″ Circuits and Systems, 2007. MWSCAS 2007. 50th Midwest Symposium on 5-8 Aug. 2007 Page(s):441 – 444.

[3] Seok-Ju Yun, So-Bong Shin, Hyung-Chul Choi, Sang-Gug Lee, “A 1mW current-reuse CMOS differential LC-VCO with low phase noise,” Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International10-10 Feb. 2005 Page(s):540 - 616 Vol. 1.

[4] N. Oh and S. Lee, "Current Reused LC VCOs," IEEE Microw. Wireless Compon. Lett., vol. 15, no. 11, pp. 736-738, November 2005.

[5] Tae-young Choi, Hanil Lee, Linda P.B. Katehi, Saeed Mohammadi, “A Low Phase Noise 10 GHz VCO in 0.18μm CMOS Process,” 2005 European Microwave Conference Publication Date: 4-6 Oct. 2005, Vol. 3, On page(s): 4 pp.

[6] Zheng Gu, Bemd Bartsch, Andreas Thiede, Rui Tao, Zhi-Gong Wang, “Fully integrated 10GHz CMOS LC VCOs”, Proc. Of European Microwave Conference, 2003, pp. 583-586.

[7] A. Ravi, K. Soumyanath , L. R. Carley , R. Bishop., “An integrated 10/5 GHz injection-locked quadrature LC VCO in a 0.18pm digital CMOS process,” Proceedings of ESSCIRC 2002 Conference, pp. 543-546.

[8] Meng-Ting Hsu; Chien-Ta Chiu, “A Low Power 10 GHz Current Reused VCO Using Negative Resistance Enhancement Technique,” Microwave Conference, 2009. APMC 2009. Asia Pacific ,Publication Year: 2009 , Page(s): 2276 – 2279.

[9] Meng-Ting Hsu; Wu-Hsueh Lin, “A low power 10GHz voltage-controlled oscillator with modified current-reused configuration,” Microwave Conference Proceedings (APMC), 2010 Asia-Pacific Publication Year: 2010 , Page(s): 578 – 581.

[10] D.Han and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," IEEE J. Solid-State Circuits, vol. 36, pp. 896-909, June. 2001.